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as of 09-Jan-2019

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Major Goals: The Hot Electron Transistor (HET) is one of the most promising electron devices to achieve power generation beyond the operating frequencies of state-of-the-art high electron mobility transistors (HEMTs) and bipolar transistors. In an HET, ultra-thin base electrodes enable ultra-short transit time with the potential to achieve THz operation. Graphene, the thinnest known conductive membrane, has a great potential as the base material in HETs. At the same time, GaN has already been established as the best material for high frequency amplification due to its wide bandgap, excellent transport properties and high breakdown field. The main objective of the Terahertz Nitride Source (TNS) project is to study the transport physics and opportunities of graphene/GaN hot electron transistors in potential THz electronic applications. In addition, the project has also produced important advances is materials synthesis and characterization, as well as numerous other device structures.

Accomplishments: Summary of project highlights

Material growth, transfer, and characterization
- First large-area CVD growth of 2H [1] and 1T' MoTe2 [2].
- Development of novel ethyl vinyl acetate (EVA) based transfer technology for two-dimensional materials [3].
- Study of the vertical transport of several layered materials and their heterostructures for the first time (i.e. graphene/MoS2, graphene/WSe2, MoS2/WSe2, SnS2/WSe2, MoS2 /MoTe2) [4-6].
- Development of state-of-the-art ferroelectric materials by ALD [7, 8].
- Identification of type-II band alignment of the SnS2 / WSe2 heterostructure[6].

Novel devices
- Demonstration of GaN/Graphene HET with record performance, through the development of 4 different generations of HETs [9-12].
- Demonstration of the first negative capacitance MoS2 FET with subthreshold swing less 60 mV/decade for use in ultra-low-power electronics[7].
- Demonstration of the shortest channel (7.5 nm) MoS2 transistor [13].
- First characterization of the ballistic length in lateral MoS2 transistor[13].
- First demonstration of room temperature negative differential resistance in Esaki-like MoS2/ WSe2 tunnel diodes[4].
- Demonstration of ternary logic inverter exploiting anti-ambipolar nature of the van der Waals heterostructure[4, 5].
- WSe2 vertical Schottky junction solar cell with record high Voc (~0.4 V) and power conversion efficiency (~4%)

[14].
- Development of a new gate-stack technology in GaN transistors that increases the frequency performance of GaN FETs by 20%.

New models and system-level analysis
- Development of a novel physics-based compact modeling framework to study the doped HfO2 ferroelectric materials developed during the project. This model has been applied to study both highly scaled Si MOSFETs, as well as GaN transistors and ferroelectric-based artificial neural networks (ANN) with highly scaled (Lg = 45 nm) FETs[15].

Training Opportunities: Nothing to Report

Results Dissemination: Nothing to Report

Honors and Awards: Fellow of the Frontiers of Engineering Program (US-EU) of the National Academy of Engineering 2014
PhD advisor of Sameer Joglekar, who received the 2014 Best Poster Award at the International Workshop on Nitride Semiconductors 2014
Young Scientist Best Presentation Award from the Japan Society of Applied Physics 2014
PhD advisor of Allen Hsu, who received the 2014 MTL Doctoral Dissertation Award at MIT 2014
Ruth and Joel Spira Teaching Award 2015
Elevation of IEEE Fellow 2016
Appointment as Editor of IEEE Electron Device Letters 2016
Choiseul Ranking of top 100 “Economic Leaders for Tomorrow” in Spain 2017
PhD advisor of Sameer Joglekar, who received Best Student Paper Award: 2016 International Conference on Compound Semiconductor Manufacturing Manufacturing (CS-MANTECH) 2017
Thompson Reuters Highly Cited Researcher 2016
Selected for the Choiseul 2017 Ranking of top 100 “Economic Leaders for Tomorrow” 2017
NASA Group Achievement Award for the “Nanotechnology Incubator Team” 2017
Advisor to Ahmad Zubair, who received a 2018 Runner-up Best Student Paper Award at the 2018 Compound Semiconductor Week (CSW 2018) 2018
Selection as a Clarivate/Thompson Reuters Highly Cited Researcher (fourth year in a row) 2018
Plenary speaker at the 2018 International Workshop on Nitride Semiconductors (IWN) 2018
Co-author in best student paper Award at the 2018 IEEE International Reliability Physics Symposium (IRPS) 2018
My High School in Madrid, which happens to be the oldest high school in Spain, named the Technology Laboratory in my honor. 2018

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Participant: Tomas Palacios
Person Months Worked: 1.00 **Funding Support:**
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Person Months Worked: 12.00 **Funding Support:**
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Terahertz Nitride Source

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Executive Summary

The Hot Electron Transistor (HET) is one of the most promising electron devices to achieve power generation beyond the operating frequencies of state-of-the-art high electron mobility transistors (HEMTs) and bipolar transistors. In an HET, ultra-thin base electrodes enable ultra-short transit time with the potential to achieve THz operation. Graphene, the thinnest known conductive membrane, has a great potential as the base material in HETs. At the same time, GaN has already been established as the best material for high frequency amplification due to its wide bandgap, excellent transport properties and high breakdown field. The main objective of the *Terahertz Nitride Source (TNS)* project is to study the transport physics and opportunities of graphene/GaN hot electron transistors in potential THz electronic applications. In addition, as it will be discussed below, the project has also produced important advances is materials synthesis and characterization, as well as numerous other device structures.

Graphene-base HETs were theoretically proposed in 2012 for potential THz applications. However, the initial experimental demonstrations suffered from low current density ($\sim\mu A/cm^2$ much lower than the theoretically predicted $\sim MA/cm^2$) and low gain ($\sim 10^{-4}$). The TNS project has focused on identifying the fundamental challenges of the graphene-base HET and overcoming those through scientific understanding.

The HET device is made of two back-to-back diodes (base-emitter and base-collector). In the base-emitter diode, the barrier and substrate materials need to be optimized to achieve high injection current density through quantum mechanical tunneling. At the same time, the emitter barrier was designed through four different generations of HETs by using transport and C-V studies.

Monolayer graphene has been the base material used throughout the project. Initial theoretical predictions in the literature were based on ideal graphene with the best materials properties. In practice, the electrical properties of a graphene film critically depends on the growth and transfer technique. The TNS project explored novel graphene and hBN growth techniques and developed a new ethyl vinyl acetate (EVA) based transfer technology which shows significantly higher graphene mobility and cleaner surface than conventional PMMA based graphene transfer method. The developed method also showed improved sidewall coverage and hence, improved the yield of the fabrication process. In addition to graphene, other two-dimensional materials like semiconducting 2H-MoS_2, 2H-$MoTe_2$ and metallic 1T'- MoS_2 and 1T'-$MoTe_2$ have been explored as potential candidates for the base of the HET. Although, integrating these materials in the base layer of the HET may lead to interesting physics, the material quality needs to improve significantly to render THz frequency operation. However, these studies led to several key scientific findings and proof-of-concept demonstrations, including the demonstration of the shortest channel (7.5 nm) MoS_2 transistor, characterization of the ballistic length in lateral MoS_2 transistors, and the first large-area CVD growth of 2H and 1T' $MoTe_2$.

Thanks to the TNS project, we identified that the base-collector junction is the major roadblock to achieve high current density and gain in graphene-base HET. Graphene is a two dimensional and inert material and lacks out of plane bonds which makes the growth of any material on top of graphene extremely challenging. First, we systematically explored the atomic layer deposition of ultra-thin oxides (Al_2O_3,HfO_2) on

top of graphene. However, it was identified that defects generated during ALD nucleation causes Fermi-level pinning and degrade the HET performance significantly. Moreover, the band offset of the available insulator materials (either conventional HfO_2, Al_2O_3 or two-dimensional hBN) is too large (1.5-3 eV) and leads to significantly large quantum mechanical reflection of the injected hot electrons in the base. This reflection drastically reduce the gain of the HET. TNS invented an alternative approach that uses a graphene/semiconductor heterojunction as the base-collector junction.

Just like with the deposition of ALD materials on graphene, the synthesis of graphene/semiconductor junctions is challenging due to the lack of dangling bonds in two-dimensional materials. To overcome this, TNS took advantage of the van der Waals interlayer bonding of layered materials and used graphene/MX_2 (M= Mo, W; X= S, Se, Te) van der Waals heterojunctions for the first time. TNS studied vertical transport of several layered materials and their heterostructures for the first time (i.e. graphene/MoS_2, graphene/WSe_2, MoS_2/WSe_2, SnS_2/WSe_2, MoS_2 /$MoTe_2$ etc.) to identify the band alignment and nature of the transport. These studies identified that graphene/WSe_2 would be an appropriate Base-Collector junction with a band offset of ~0.54 eV while graphene/MoS_2 is essentially an ohmic junction that cannot be used as an effective hot electron filter. Moreover, these studies led to, i) first demonstration of room temperature negative differential resistance in Esaki like MoS_2/ WSe_2 tunnel diodes, ii) demonstration of ternary logic inverter exploiting anti-ambipolar nature of the van der Waals heterostructure, iii) identification of type-II band alignment of the SnS_2 / WSe_2 heterostructure, iv) WSe_2 vertical Schottky junction solar cell with record high V_{oc} (~0.4 V) and power conversion efficiency (~4%).

By combining all this work, the TNS project has demonstrated the integration of two-dimensional van-der-Waals heterostructure with GaN/AlN for the first time and achieved record performance for single-atom-thick base HETs. In the most advanced devices fabricated in the project (Generation 4), a 2-nm-AlN tunnel barrier grown on bulk n-GaN acts as hot electron injector for the HET. The ultra-low density of threading dislocations in bulk GaN wafers, ensures the large breakdown voltage and low leakage current of the AlN tunnel barrier. Due to the large polarization difference between AlN and GaN, the AlN/GaN heterostructure has high 2-DEG concentration with a relatively thin barrier thickness compared to AlGaN/GaN. This 2-DEG concentration provides high emitter current density. In addition, the use of a Schottky barrier as the base-collector barrier, instead of the traditional thin oxide layer, improves the injection efficiency ($\alpha = I_C/I_E$) of the device significantly. The resultant structure shows collector current density ($\boldsymbol{J}_C$) of 3 kA/cm^2 and gain ~5-7, which is significantly higher than in any other graphene-based HET, although still slightly below the world's best all-GaN HET (46 kA/cm^2 and a gain of 14.5).

In addition to HETs, TNS has been exploring novel ideas to enhance the f_T and f_{max} of the state-of-the-art GaN HEMTs. A novel physics-based compact modeling framework has been developed to study the doped HfO_2 ferroelectric materials developed during the project. Using Landau-Khalatnikov theory of ferroelectrics, it has been identified that the frequency and gain of the GaN HEMTs can increased up to 20% using ferroelectric in the gate stack of the RF MISHEMTs. TNS has also developed an integration technology that allows the use of these ferroelectric materials in conventional GaN and InGaAs HEMT structures. Finally, the compact model has been extended to capture the memory behavior

of the ferroelectrics using Preisach model and voltage dependent switching transient model. The developed model has been used to the study the device and system level performance of artificial neural network (ANN) with highly scaled (L_g = 45 nm) FETs with ferroelectric gate dielectric. The model shows that ANN developed with optimized device geometry can achieve 88-90% accuracy of in classification of 1 million MNIST handwritten digits with very low latency and energy dissipation.

Finally, although it was found that ALD dielectrics were not suitable for HETs, the scientific learning from this ALD study has allowed the development of high quality ALD doped HfO_2 ferroelectric thin films and led to the first demonstration negative capacitance MoS_2 FET with subthreshold swing less 60 mV/decade.

Summary of project highlights

Material growth, transfer, and characterization

- First large-area CVD growth of 2H [1] and 1T' $MoTe_2$[2].
- Development of novel ethyl vinyl acetate (EVA) based transfer technology for two-dimensional materials [3].
- Study of the vertical transport of several layered materials and their heterostructures for the first time (i.e. graphene/MoS_2, graphene/WSe_2, MoS_2/WSe_2,SnS_2/WSe_2, MoS_2 /$MoTe_2$) [4-6].
- Development of state-of-the-art ferroelectric materials by ALD [7, 8].
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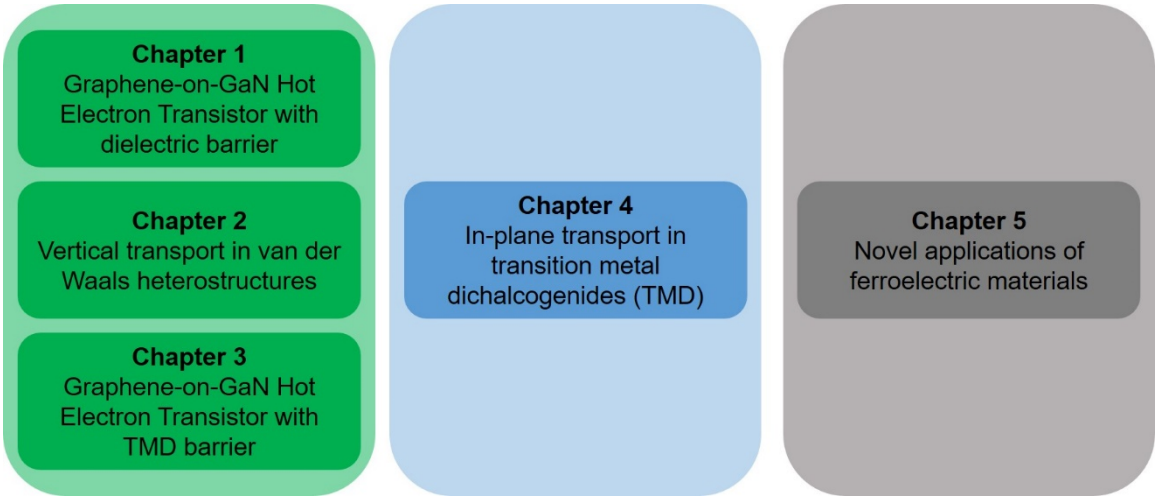
Organization of the report

The report is divided into five different chapters. In chapter 1, we discuss the motivation, challenges and design-space of the graphene-on-GaN HETs with oxide collector barrier. We discuss the need for the development of graphene/semiconductor base-collector junctions. The fabrication of high quality graphene/semiconductor junctions is challenging and transport (in-plane and out-of-plane) in semiconducting 2D materials has not carefully been studied in the literature. In chapter 2, we present the fabrication and characterization methodology of out-of-plane tunneling transport across the semiconducting 2D materials based van der Waals heterojunctions (MoS_2/WSe_2). The understanding developed in this chapter has been used to design a new generation high performance HETs presented in chapter 3. Here we have integrated MBE grown GaN/AlN tunneling emitter and graphene/WSe_2 van der Waals heterojunction diodes. In chapter 4, we present the in-plane transport study and scaling limit of semiconducting 2D materials using MoS_2FET as a case study. Chapter 5 discusses a novel class of material, ferroelectric HfO_2, which was developed thanks to the scientific understanding achieved in chapter 1. In this chapter, we also present our physics based compact model and three novel applications using ferroelectric HfO_2 – negative capacitance for overcoming Boltzmann limit of 60 mV/decade in FETs (experimental demonstration), high-frequency devices with improved performance and artificial neural network with highly scaled (L_g= 40 nm) FeFETs.

Organization of the report



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1 GRAPHENE-ON-GaN HOT ELECTRON TRANSISTOR WITH DIELECTRIC BARRIER

The concept of a high performance vertical unipolar transistor with ballistic transport has been in the semiconductor community over many decades since the initial proposal of tunnel emission device by C.A. Mead[16]. The device was later termed as hot electron transistor (HET)[17]. The HET is a unipolar and majority carrier device where the base-to-emitter voltage controls the transport of ballistic hot electrons through a transit layer smaller than the mean free path (λ_{mfp}) of the carriers. Hence, HETs have the potential to exhibit higher frequency performance than HBTs, which are limited by the diffusion of minority carriers across the base, and HEMTs, which are limited by the saturation velocity of carriers and the lithography of the gate[16].

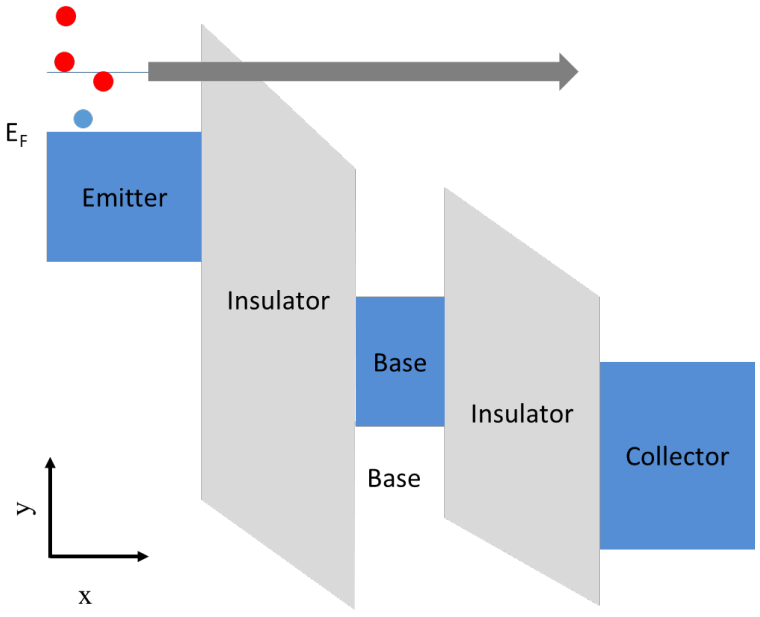


Figure 1 Schematic energy band representation of a tunnel emission device[16] . Here x-axis represents the depth along the out-of-plane transport direction and y-axis represents the energy.

Figure 1 shows the schematic representation of the energy band diagram of the tunnel emission device. In this device, the E-B insulator works as tunnel emitter and the B-C insulator works as the collector barrier. The base layer sandwiched between these two insulators works as the highly conductive transport layer to facilitate high speed transport. The success of this structure critically depends on the ability to grow a defect, pin-hole free highly conductive base layer thinner than mean free path of the injected carriers. Due to technological limitations to grow such a layer, the gain in this device has been limited for a long time to 0.01-0.1[16].

1.1 Operation of a Hot Electron Transistor

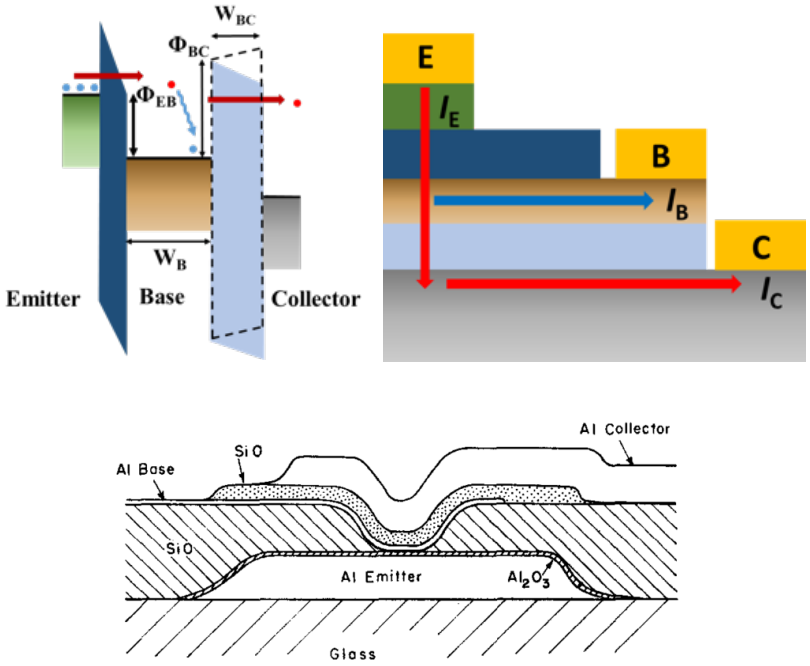


Figure 2 (a) Schematic energy band diagram of a HET with an insulator-collector barrier along the vertical direction in the on-state for $V_{CB} > 0V$ (solid line) and $V_{CB} < 0V$ (dotted line), showing the carrier flow direction and relevant design parameters. (b) Cross-section and the direction of carrier flow in HET. (c) Cross section of typical Al/Al_2O_3 (5-10 nm)/Al (30 nm)/SiO (10 nm)/Al tunnel emission device with Al base used in [16].

As shown schematically in Figure 2, a typical HET structure consists of a hot electron injector (emitter/emitter-barrier stack), a transport layer (base) and a hot electron analyzer or filter (collector-barrier/collector-stack). The HET can be considered as a combination of two back-to-back diodes connected in series, namely the E-B diode and the B-C diode. Under the typical operating conditions, the emitter-base (E-B) diode is forward biased ($V_{BE} > 0$ V) and electrons are injected into the base with an excess energy above the Fermi energy of the base ($eV_{BE}-E_f$). If the base-collector (B-C) diode is then reverse biased ($V_{CB} > 0$ V), it will allow the hot electrons reaching the base to travel to the collector with minimal scattering (quasi-ballistically) (Figure 1a). However, if $V_{CB} < 0$ V,the energy barrier for the base electrons (shown by the dotted lines in Figure 1a) will increase and majority of the injected electrons will thermalize in the base by scattering and quantum mechanical reflection, and eventually contribute to the base leakage current. Several material systems have been used for HET development including metal thin films[16, 18], non-polar III-V semiconductor heterostructures [19-22], complex oxides[23], and superconducting materials[24]. The lack of success in the tunnel emission devices with metal base appeared to be a major roadblock until Shannon[17] proposed the use of semiconducting base layer with degenerate doping. This structure adopted the so-called semiconductor-metal-semiconductor (SMS) configuration where the emitter-base diode was a Schottky junction. The search for a high performance HET continued thanks to the rapid success of GaAs growth technology. There have been several demonstration of GaAs-based HET or tunneling hot electron transistor amplifier (THETA) but most of these devices worked only in cryogenic temperatures[19]. This is partially due to the fact that the band offset in III-V non-polar semiconductor materials is relatively small. In the device with GaAs base

regions[25] used so far , the injected hot electrons are thermalized in the base as a result of inelastic (intra- and inter-valley[22] electron–electron, electron–phonon) and elastic (impurities) scattering. Therefore, the demonstration of high performance HETs has been limited by the technological inability to scale the base thickness below the λ_{mfp} of the carriers, and electrostatic decoupling the collector from the emitter. The first GaAs HETs to have current gain (β >10) at room temperature were demonstrated by Levi et al.[26].

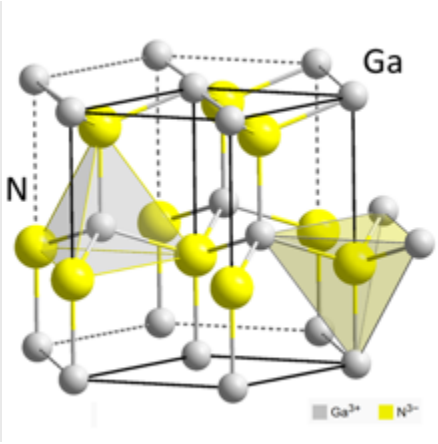


Figure 3 Crystal structure of wurtzite GaN.

The success of the wide bandgap III-N materials family (GaN, InN, AlN and their heterostructures) enabled many exciting and revolutionary applications in solid-state lighting, power and high frequency electronics due to their unique crystal structure and material properties. In electronic devices, GaN and related heterostructures have found unprecedented success due to their high breakdown fields and the presence of two-dimensional electron gas, which leads to high carrier density. At the same time, the large band offset and large inter-valley separation in this material systems can also be used for high performance HETs as proposed by Shur in 2000[27].

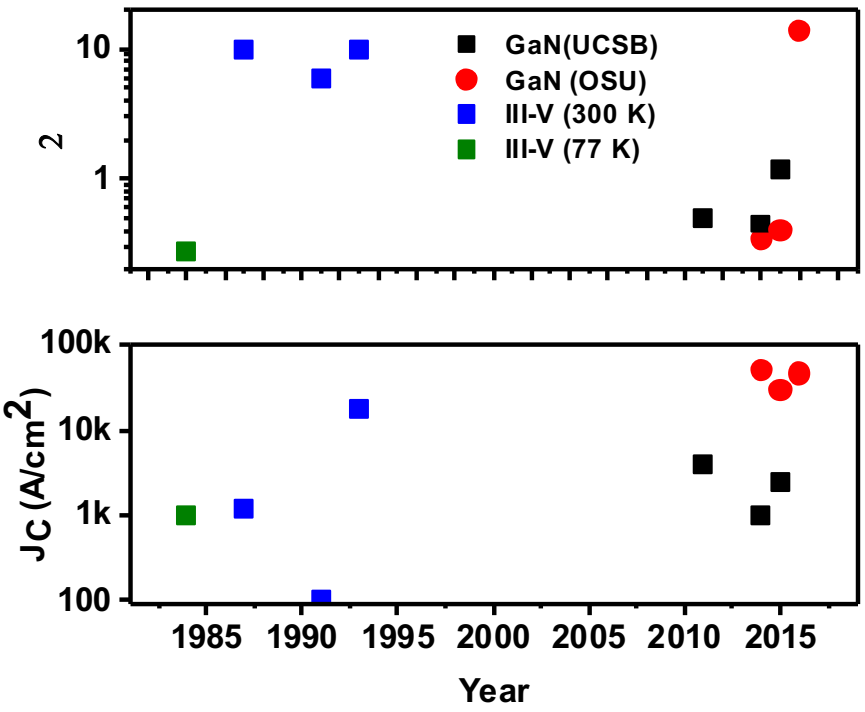


Figure 4 Chronological evolution of experimentally demonstrated HET performance over the years [28-44].

Dasgupta et al [28] experimentally demonstrated the first GaN HET where thermionic emission from GaN/AlGaN heterostructures was used as emitter. Although the device had high current density (~5 kA/cm^2) at room temperature, it suffered from low current gain (β<1). However, this demonstration started a new era of HET development and after 15 years of theoretical proposal, Gupta *et al*.[36] demonstrated the first GaN HET with β>1 using a GaN/AlN tunneling emitter. Thanks to further optimization of growth and structural parameters, Yang *et al*. demonstrated HET with excellent current gain (>10)[43] and current density (~46 kA/cm^2)[36, 43] at room temperature with 2.5 nm AlN tunneling emitter and 8 nm heavily doped GaN base. Figure 4 shows the evolution of GaN HET performance over time. Although GaN HETs have enjoyed tremendous success in performance, the growth of an ultra-scaled base layer still remains a challenge.

1.2 The concept of Graphene-base HET

Single atomic layer two-dimensional (2D) materials are naturally suitable for applications requiring ultra-thin, defect-free films. Several vertical tunneling devices[45] for both logic (tunneling transistors[46], barristors[47]) and high frequency applications (resonant tunneling device[48]) have been demonstrated using these materials. Monolayer graphene, with ultra-high mobility and a dangling-bond-free inert surface, is an ideal candidate as a low resistance, scattering-free base material in HETs, as it can overcome the growth-related limitations of bulk semiconductors. Theoretical studies have predicted that with an optimized structure, a maximum unity gain operating frequency (f_T) up to several THz[49-53], I_{on}/I_{off} over 10^5 and high current gain[51, 54, 55] can be achieved in graphene-base HETs (GHET) or graphene-base transistors (GBT). An alternative, thermionic emission based structure, the graphene base heterojunction transistor (GBHT) [50] has also been proposed with similar high frequency performance[56]. Figure 5 benchmarks the theoretically predicted high frequency performance of these devices using monolayer graphene as the base layer against several state-of-the-art high frequency devices. Although the graphene and in general two dimensional materials technology was in very early stage, these theoretical predictions inspired a new generation of HET development. Vaziri *et al.[57]* and Zeng *et al*. [58] experimentally demonstrated the first graphene-base hot electron transistor with a Metal-oxide-metal-oxide-metal (MOMOM) configuration similar to original tunnel emission device proposed by Mead using Si/SiO_2

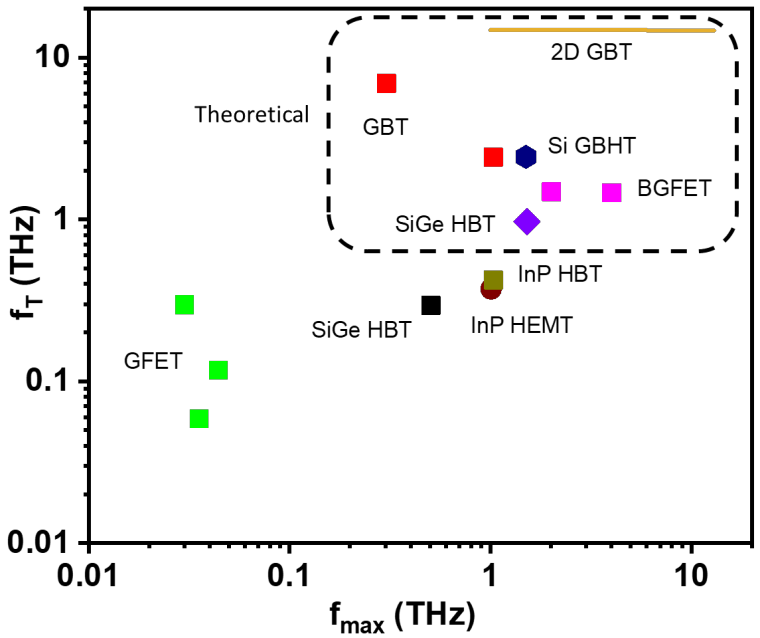


Figure 5 Theoretically predicted high frequency performance of graphene base transistors (Si GBT[51], GBHT[50], 2D GBT[59], BGFET[60]) benchmarked against state-of-the-art theoretical (SiGe HBT[61]) and experimental (GFET[62], SiGe HBT[63], InP HBT[64], InP HEMT[65])RF devices(adapted from [66]).

tunneling emitter barrier and atomic layer deposited high-$\varkappa$ Al_2O_3 or HfO_2 as the collector barrier. The initial experimental demonstrations [57, 58, 67, 68] showed successful operation in terms of current modulation (on-off ratio $>10^5$) but suffered from low output current density ($\sim\mu A/cm^2$), low current gain, low injection efficiency, low output impedance and high threshold voltage.

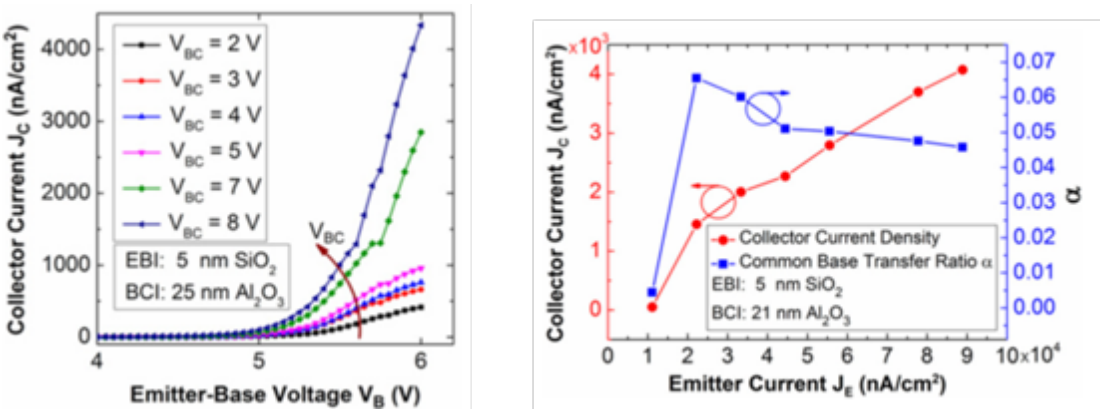


Figure 6 Transport and gain characteristics of first graphene-base HET[57].

1.2.1 Design space of graphene-base HET (GHET)

The initial demonstrations of GHETs were focused on the ultimate scaling of base thickness using monolayer graphene. However, to understand its full potential and improve its performance towards the projected theoretical estimation it is important to divide this complex device into fundamental design blocks. In this project, the GHET structure has been divided into two fundamental building blocks as shown in Figure 7 and each block has been studied separately. After understanding each component, the optimized blocks have been integrated to achieve a high performance graphene-base hot electron transistor. In addition to the development of high performance HETs, the findings in each stage of this project have enabled a number of breakthrough technologies, proof-of-concept demonstration and scientific understanding in two dimensional materials electronics which will be thoroughly discussed in the following chapters of this report.

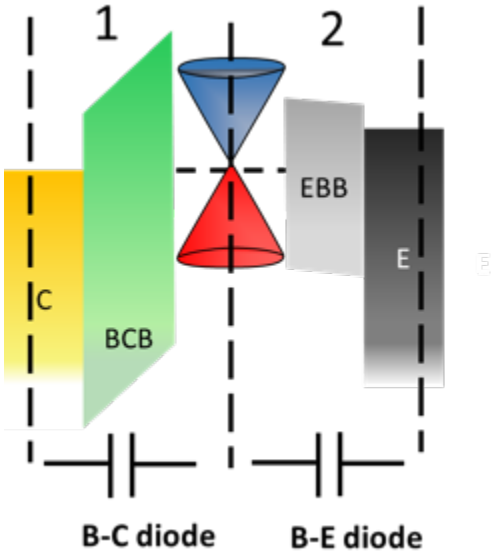


Figure 7 Schematic representation of the fundamental building blocks of GHET.

1.2.1.1 First generation GaN/Graphene HET

The first design consideration for the development of GHET is to select the suitable substrate or host material. Conventional HETs have been built using a double mesa emitter-up structure as shown in Figure 2, where the collector layer is typically the substrate material. Advanced growth techniques like molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) enable the high quality growth of subsequent collector barrier layers, ultra-thin base and emitter barrier layers. The growth techniques of 2D materials are not mature enough to enable such high quality precision growth and the device demonstrations so far are mostly based on mechanically-exfoliated flakes. Moreover, the subsequent growth of high quality thin layer materials on top of graphene and other 2D materials is extremely challenging as it will be discussed later. To overcome these technological limitations, the HETs presented in this project use a collector-up

structure where the high quality emitter barrier is grown on the substrate before introducing graphene in the system.

One of the major shortcomings of the GHETs reported so far is the low output current density, which can be increased by improving the i) emitter current (I_E) and ii) injection efficiency or base transport factor, defined by:

$$\alpha = \frac{I_C}{I_E},$$

as shown in the band diagram in Figure 2, the quantity I_E is dominated by the quantum mechanical tunneling of electrons and thermionic emission from the emitter to the base. According to the WKB approximation, the tunneling probability (T) through a barrier can be defined as:

$$T \propto e^{-\gamma},$$

where γ is a function of both the barrier thickness and height. Hence, the emitter current can be significantly increased by scaling the barrier thickness[68]. However, the initial graphene HETs suffer from a low injection current density from the emitter through the emitter-base barrier due to the thick oxide layers (>5nm SiO_2) typically used as the emitter-base barrier [57, 58] on top of heavily doped Si emitter. The choice of SiO_2 is dictated by the fact that it can form defect and trap-free interface with Si which is critically important for tunneling. The tunneling barrier height of these structures is defined by the conduction band offset (for n-type device) between Si and SiO_2 which is 3.1eV. However, this large barrier height limits the probability of tunneling as well as the injection current density.

GaN materials system offers several advantage in designing emitter for GHETs. First, due to non-centrosymmetric nature of the crystal structure it has spontaneous polarization. This allows for GaN heterostructures to have a high density (up to $10^{13}/cm^2$) two-dimensional electron gas (2-DEG) at their interface. The presence of a 2-DEG eliminates the need for doping the emitter, which can reduce parasitic capacitances and improve the material quality. Second, the conduction band offset for $GaN/Al_xGa_{1-x}N$ or $GaN/In_xAl_{1-x}N$ heterostructure can be tuned by simply controlling the mole fraction of Al in the heterostructure. Finally, GaN power and optoelectronic devices are mature and mainstream industrial technology. As a result, high performance GHETs built on GaN could seamlessly be integrated with other commercial technologies.

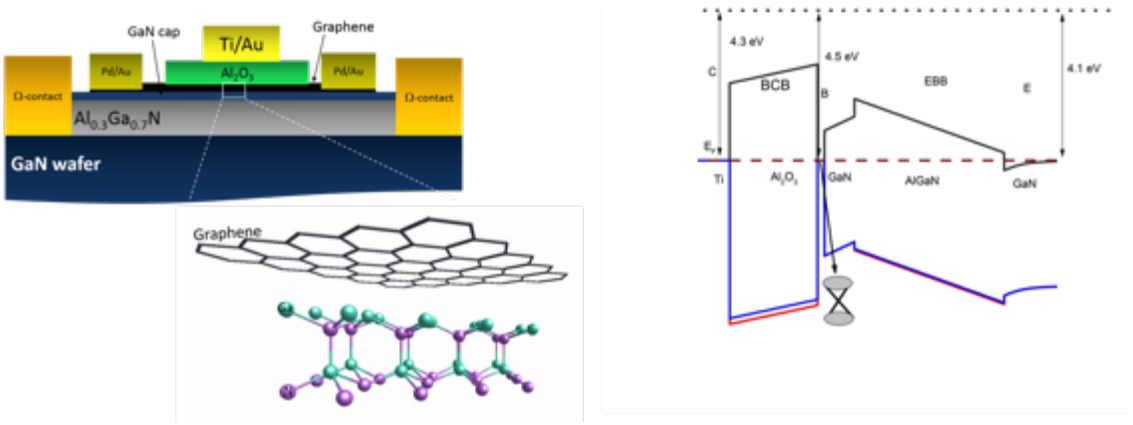


Figure 8 Schematic cross section and energy band diagram of the 1st generation GHET developed in this project.

Figure 8 shows the schematic cross section and energy band diagram of the 1st generation graphene-on-GaN HET fabricated in this project. In this structure, a GaN/$Al_{0.3}Ga_{0.7}N$ (15-18 nm) heterostructure has been used as emitter stack while ALD grown Al_2O_3 (10-15 nm) was used as collector barrier.

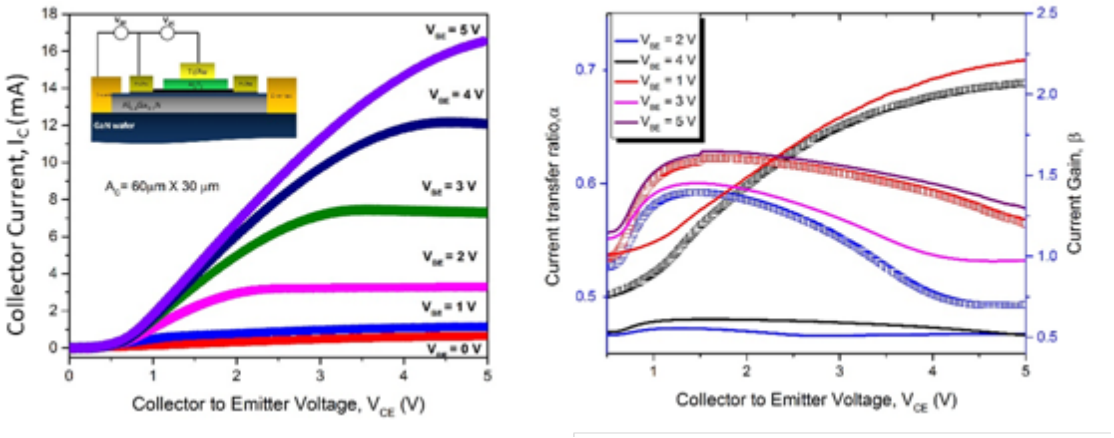


Figure 9 Output and gain characteristics of the 1st generation GHET.

The initial graphene-on-GaN HET shows orders of magnitude higher current than GHETs built on Si (β ~10^4) [57] but the maximum gain of these devices is limited to 2. The low gain can be attributed to the use of thick Al_2O_3 as the collector base barrier which also has a large ΔE_c with graphene. This large ΔE_c, when combined with a thick tunneling barrier, can lead to large quantum mechanical reflection of the injected hot electrons as the base-collector interface and hence the hot electrons scatter and relax. These cold electrons contribute to the base leakage current rather than to the collector current, and reduce the gain of the device. Moreover, the carrier injection from the emitter is a combination of both tunneling and thermionic emission, which is not favorable for scattering free transport

in the base. To overcome these above mentioned limitations the thickness of the both emitter and collector barriers should be reduced significantly.

1.2.1.2 Emitter/Emitter base barrier stack

It has been established in the previous section that to enhance the tunneling injection from GaN emitter to graphene base, the barrier separating these two layers (i.e. AlGaN) needs to be scaled down. The reduction of tunneling barrier thickness in GaN/AlGaN heterostructure leads to another complication. The 2-DEG density drops significantly with thickness scaling of the AlGaN layer as shown in Figure 10. Alternatively, a GaN/InAlN

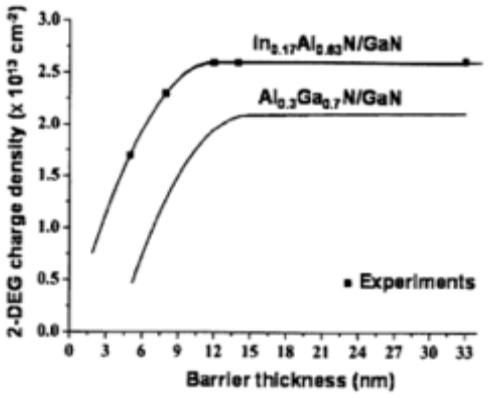


Figure 10 Calculated 2-DEG density as a function of barrier thickness.

heterostructure can be used instead of a GaN/AlGaN emitter stack. InAlN with 17% In is lattice matched with GaN substrate, and it can have large (>10^{13}/cm^2) 2-DEG density when scaled below 5 nm thickness. To study the effect of barrier scaling, GaN/InAlN/graphene tunnel diodes have been fabricated. These devices were fabricated on HEMT structure wafers grown by IQE with different InAlN barrier thickness.

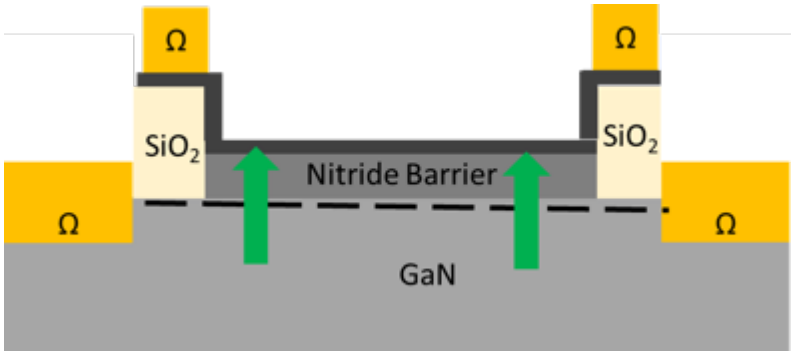


Figure 11 Schematic cross-section of base-emitter (B-E) diode.

Figure 11 shows the cross section of the base-emitter diode fabricated to study the effect of emitter barrier thickness. Four different epitaxial structures were evaluated:

- 3nm GaN/10.6 nm AlGaN/GaN (reference)
- 7.4 nm InAlN/ 1 nm AlN/12 nm GaN/$In_{0.15}Ga_{0.85}N$
- 7.4 nm InAlN/ 1 nm AlN/ 3 nm GaN/InGaN
- 5nm InAlN/1 nm AlN/GaN

The device fabrication starts with mesa isolation of 2-DEG in reactive ion etching with BCl_3/Cl_2 chemistry. The ohmic contact is then formed by Ti/Al/Ni/Au alloyed with rapid thermal annealing at 800°C. To avoid parasitic leakage path between base contact and 2-DEG, 100-200 nm thick PECVD SiO_2 with TEOS precursor has been deposited and patterned to define the device active area. This SiO_2 isolation layer ensures the conduction is limited to the active area as shown by green arrow. After defining active area, large area monolayer CVD graphene has been transferred. The challenges associated with graphene transfer will be discussed later. Finally, graphene layer is patterned and ohmic contact is formed by ebeam evaporation of metal.

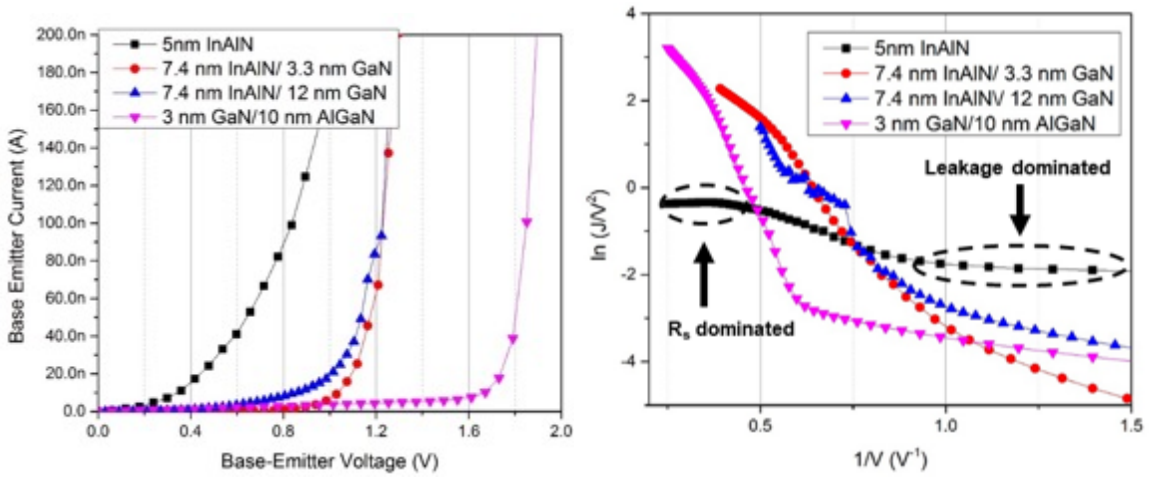


Figure 12 (a) Diode turn-on and (b) Fowler-Nordheim tunneling characteristics.

Figure 12(a) shows the diode turn-on characteristics of fabricated B-E diodes. The turn-on voltage of the diode scales with the barrier thickness. Moreover, to verify the tunneling injection, the characteristics have been plotted using Fowler-Nordheim (F-N) formulation ($\ln (J/V^2)$ vs 1/V). The linear region in the F-N plot corresponds to the tunneling [35, 68]. Figure 12(B) shows that the F-N plot of all diodes can be divided into three regions. The left region of the plot corresponding to low bias region and it is dominated by leakage, while the right region at higher bias is dominated by the series resistance. As expected, the onset of tunneling is a function of the barrier thickness, which increases with barrier thickness. To further understand the diode behavior, the capacitance voltage characteristics have also been studied.

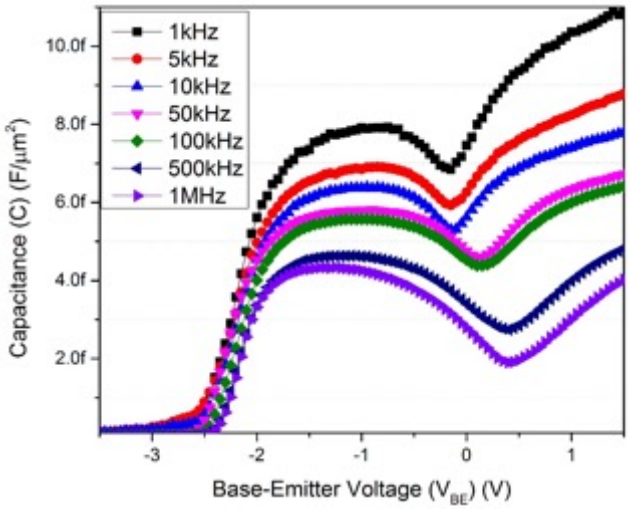


Figure 13 C-V characteristics of a typical B-E diode.

Graphene has a finite density of states (DoS) near the Dirac point unlike metal. The quantum capacitance is proportional function of DoS. Quantum capacitance of the graphene can significantly affect the device electrostatic under bias due to the finite nature of the DoS. The Fermi energy level of graphene shifts under bias which changes the electric field across the barrier. This quantum capacitance can lead to incomplete screening of electric field and hence, degrade the device characteristics for thin tunneling barrier. Figure 13 shows the C-V characteristics of a typical B-E diode at different frequencies. The C-V characteristics loos similar to the ones in regular GaN MIS capacitors from negative bias to -1V bias. At large negative bias, the 2-DEG is depleted and hence the total capacitance is lower. As the applied bias increases, capacitance increases towards accumulation. However, at higher bias a local minima appears in the capacitance, which is due to quantum capacitance effect. The local minima corresponds to the Dirac point of the graphene layer. To further confirm the fact that this local minima is due the quantum capacitance of the graphene, the sample is annealed in the forming gas ambience. The graphene is typically

p-doped due to physio-absorbed molecules in the ambient condition. Forming gas annealing usually removes the physio-absorbed molecule and make the graphene less p-doped, which shifts Dirac point towards more negative voltage. The C-V characteristics after annealing confirms this behavior as the local minima has been shifted to more negative bias. This expected behavior of graphene quantum capacitance confirms the existence of a high quality interface between graphene and GaN, which is a prerequisite of high performance tunneling device.

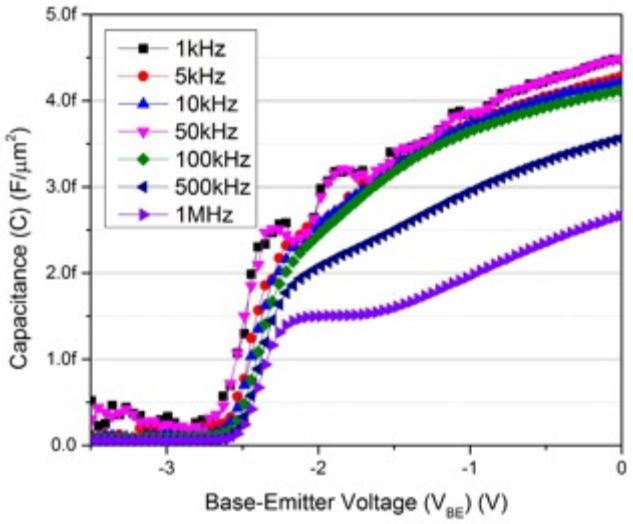


Figure 14 C-V characteristics of the diode shown in Figure 13 after annealing.

In summary, a fabrication technology has been developed for high quality GaN/InAlN/graphene tunnel diodes, and tunneling has been confirmed from the F-N plots. The tunneling current density achieved at V_{BE} =2V is 10 A/cm^2, which is higher than best reported Si/Oxide/graphene tunnel diode at the same bias[68]. This current density is still not enough to achieve high performance HET and further scaling of tunnel barrier thickness is required. Similar to the AlGaN barrier case, further scaling on an InAlN barrier would

significantly decrease the 2-DEG density. Moreover, reverse leakage in AlGaN and InAlN-based barriers due to random alloy fluctuation can be an issue[31]. One possible solution is to use GaN/AlN heterostructure as the emitter of GHET.

Narrower AlN-based tunneling barriers would improve the tunneling probability and also allow a lower turn-on voltage, which would enable the low voltage operation of the device, currently absent in existing HETs (with $V_{BE} > 2$ V). Our third generation of devices (Figure 22) use ultrathin AlN on GaN as the emitter stack. The use of all-binary heterostructures eliminates leakage current due to percolation transport arising from random alloy fluctuation[31], while the large polarization difference between GaN and AlN enables a very high 2-DEG density in the GaN-side of the heterostructure, which allows for low emitter resistance. Moreover, GaN/AlN heterostructure has higher tunneling current than Si/SiO_2 due to smaller conduction band offset at the junction. The epitaxial nature of the AlN/GaN also provides high quality trap-free interface.

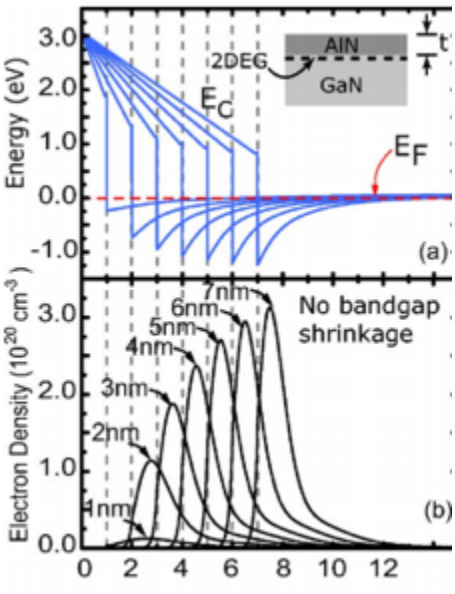


Figure 15 Calculated (a) energy band diagram and (b) 2-DEG density GaN/AlN heterostructure (adapted from [69]).

Figure 15 shows that high 2-DEG density can be achieved for ultra-thin AlN grown on GaN substrate which will be used in the devices discussed in chapter 4.

1.2.1.3 Collector/collector base barrier stack

The optimization of the emitter tunnel barrier can improve the current density injected into the base from the emitter. However, to improve the output current density, the common-base injection efficiency, α, should be close to unity. α can be expressed as:

$$\alpha = \alpha_B \alpha_{BC} \alpha_C$$

where α_B, α_{BC} and α_C represents base efficiency, base-collector barrier filtering efficiency and collector efficiency, respectively. The base efficiency is defined as:

$$\boldsymbol{\alpha_B = exp\left(-\frac{W_B}{\lambda_{mfp}}\right)}$$

where W_B is the physical thickness of the base and λ_{mfp} is the carrier mean free path. Monolayer graphene has near unity α_B because of its atomically thin nature (t= 3.4 Å), which is superior to any other bulk material. In the case of GaN, the mean free path is around 15 nm[33] and α_B will be fundamentally limited even in the case of an ultra-scaled graphene base. However, the relatively low values of α in GHETs arise from the poor filtering efficiency (α_{BC}),which will be systematically studied below.

The filtering efficiency depends on both the quantum mechanical reflection at the barrier and the tunneling conductance of the barrier. To minimize the reflection, base-collector band-offset (Φ_{BC}) should be smaller than the emitter-base band-offset (Φ_{EB}) (Figure 1a), but if Φ_{BC} is too low, then cold electron leakage from the base to the collector will be higher, which will degrade the ballistic injection efficiency.

Moreover, to efficiently tune the barrier width with an applied bias and thus modulate the tunneling probability, the barrier shape needs to be triangular rather than trapezoidal[68] as for a trapezoidal barrier, the effective barrier thickness is equal to its physical thickness.

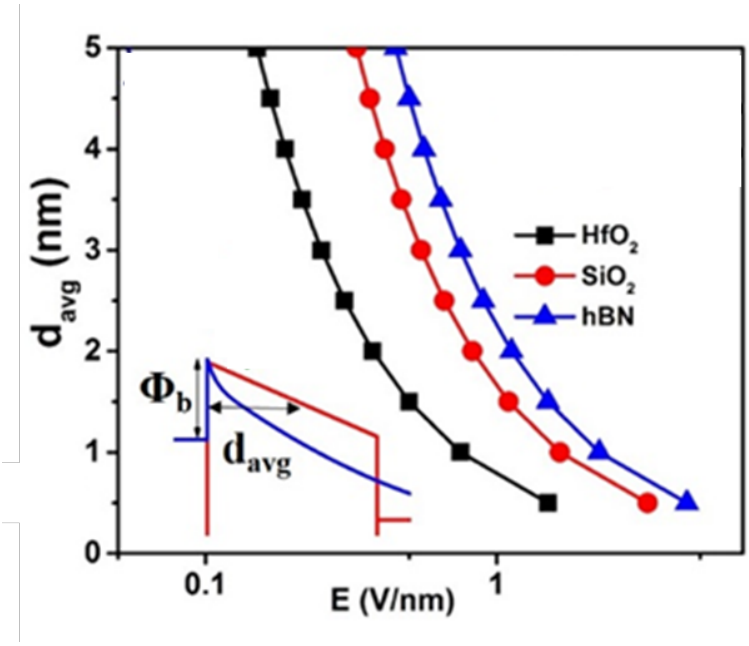


Figure 16 Average tunneling distance in graphene/Oxide junctions as a function of thickness. Inset shows the average tunneling distance comparison between a triangular and trapezoidal barrier under bias.

Figure 16 shows a comparison of the average tunnel barrier width (computed at the full width at half maximum (FWHM) of the tunnel barrier width) for different conventional dielectrics at the minimum electric field required to change the barrier to a triangular shape from trapezoidal. Owing to the large conduction band offset with graphene (that is 4.5 eV for hBN), the required electric field to achieve a particular tunnel barrier width is relatively large so the device needs to be operated at a relatively large V_{BC}, which makes it prone to breakdown. Therefore, to improve α_{BC}, the base-collector dielectric barrier has to be ultra-thin. Moreover, the base-collector junction in these devices cannot completely screen the emitter electric field, which causes severe increase in output conductance. Apart from this fact, forming ultra-thin tunneling layers on top of a graphene base is very challenging because the chemically inert, hydrophobic surface of graphene does not allow conformal nucleation of atomic layer deposition (ALD) thin film oxides [70]. Therefore, as a result, relatively thick layers of oxides (~15–55 nm) have been used so far [57, 58, 68, 71] to achieve conformal, pin-hole free barriers.

To overcome the issue, the first approach would be to develop technology for ultra-thin ALD dielectrics on top of graphene. Most of the graphene or other 2D material-based devices described in the literature use thick dielectrics (90-300 nm SiO_2) as the gate dielectric and there is lack of reports on highly scaled EOT dielectrics for this family of materials. To study the effect of highly scaled EOT dielectrics in graphene the structure

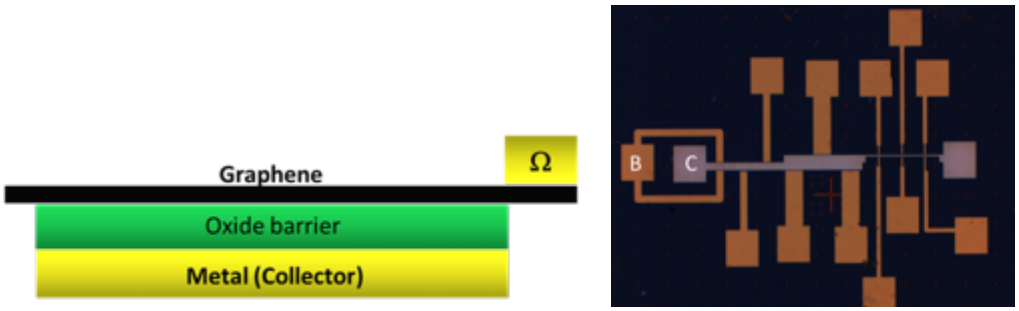


Figure 17 (a) Schematic cross section and (b) optical image of the structure used in the B-C diode study.

we fabricate the structures shown in Figure 17. Nucleation of the initial few cycles is critically important for scaled EOT high-$\varkappa$ dielectrics grown in ALD. To improve the nucleation, Al has been used as the back electrode in this study. At the beginning of the ALD growth, 10 cycles of water is pulsed into the chamber at the desired temperature for oxide growth. These water pulses forms a native Al_2O_3 on the Al surface that acts as the seed layer for subsequent ALD process.

Table 1-1 Splits used for ALD study

Oxide	Thickness	Thickness
Al_2O_3	3 nm	7 nm
HfO_2	3 nm	7 nm

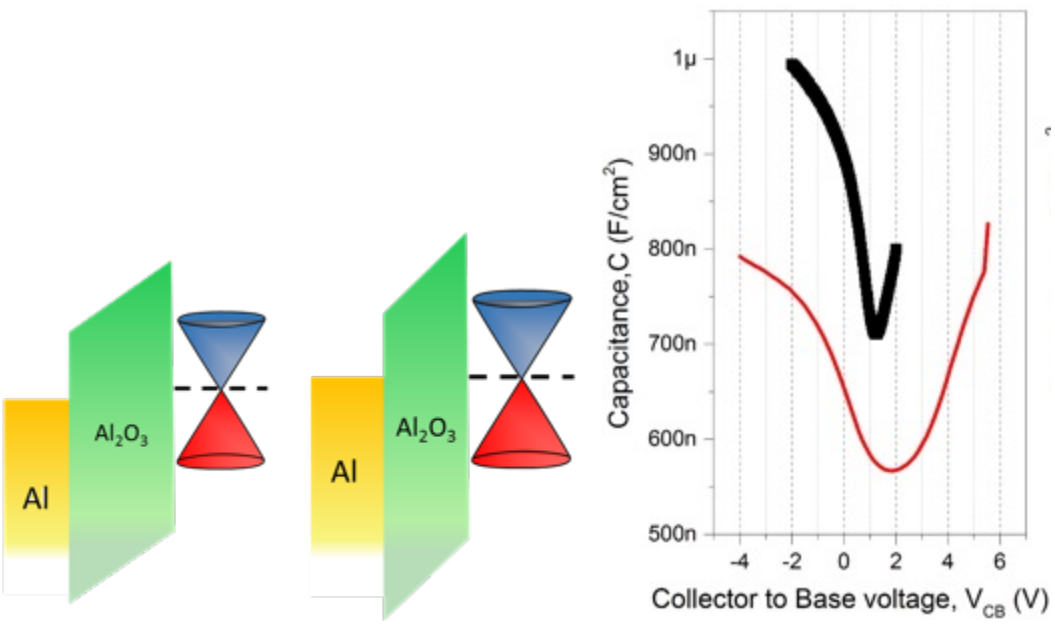


Figure 18 C-V characteristics of Al/Al_2O_3/graphene capacitor. Red and black curves represents 7 and 3-nm-thick films, respectively.

The dielectric optimization study starts with scaling down the Al_2O_3 thickness. In the 1st gen devices, a dielectric thickness of ~11 nm (100 cycle + 1 nm seed layer) was used. Figure 18 shows the C-V characterisitcs for 70 cycle and 30 cycle Al_2O_3 graphene capacitors. The effect of graphene quantum capacitance can be studied from the position of the Dirac point in these characteristics as mentioned in the previous section. The capacitance value of 3 nm dielectric capacitor is higher than 7nm which is expected from parallel plate capacitor formula. Moreover, the leakage across the dielectric starts to dominate for any bias larger than 2V. On the other hand, 7 nm dielectric can sustain -4V to 5V without having significant leakage.

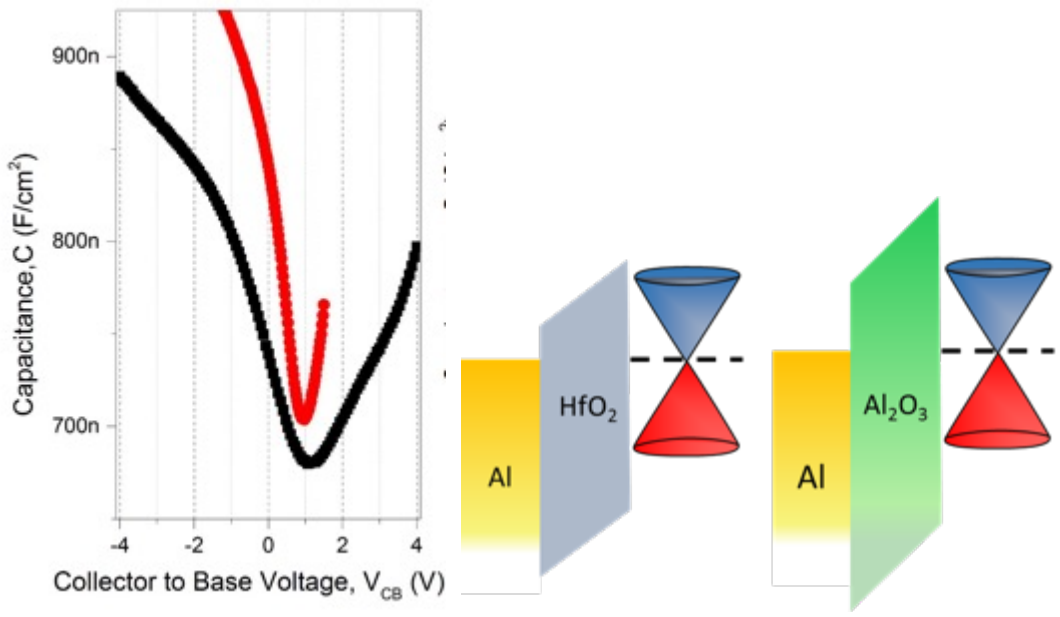


Figure 19 C-V characteristics of Al/Oxide (3 nm)/graphene capacitor. Red and black curve represents HfO_2 and Al_2O_3 respectively.

To understand the effect of the dielectric constant on the device performance, the thickness of the film is kept constant (300 cycles in ALD) for both HfO_2 and Al_2O_3. Figure 19 shows the C-V for both capacitors. The capacitance value of HfO_2 is higher due to higher dielectric constant (~25) compared to Al_2O_3 (~9). The EOT can be calculated to be 2.14 nm and 1.51 nm for to Al_2O_3 and HfO_2 respectively. The conduction band offset of the HfO_2 with graphene is much smaller than Al_2O_3 and should act better as filtering barrier in terms of carrier extraction efficiency. It should be noted that the highly scaled high-$\varkappa$ dielectric developed here can enable applications beyond HETs, like ultra-short channel MoS_2 transistors and ferroelectric HfO_2 which will be discussed in chapters 2 and 5, respectively.

After establishing the baseline scaled dielectric for a graphene capacitor, the next goal is to develop a process that can enable the growth of highly scaled dielectric of similar

thickness on top of graphene. The graphene surface is hydrophobic and chemically inert which result in poor nucleation of ALD films on it. As a result, the ALD shows island-like growth rather than conformal growth.

The use of a thin Al seed layer (< 1 nm) is the most common approach for gate dielectric growth on top of graphene or other 2D materials [70]. In this work, 0.8 nm Al has been evaporated at slower deposition rate of 0.1A/s to ensure conformal coverage on the graphene surface. After the evaporation, the sample is then transferred to the ALD chamber. The ALD chamber temperature is then raised to 250°C from idle temperature of 150°C. After the stabilizing the sample temperature at 250°C, 10 cycle of water is pulsed into the chamber. This process ensures proper oxidization of seed layer. This seeding process works well for dielectric thicker than 5 nm. However, dielectric thinner than 50 cycle shows island like growth as shown in the atomic force micrograph image of Figure 20 .

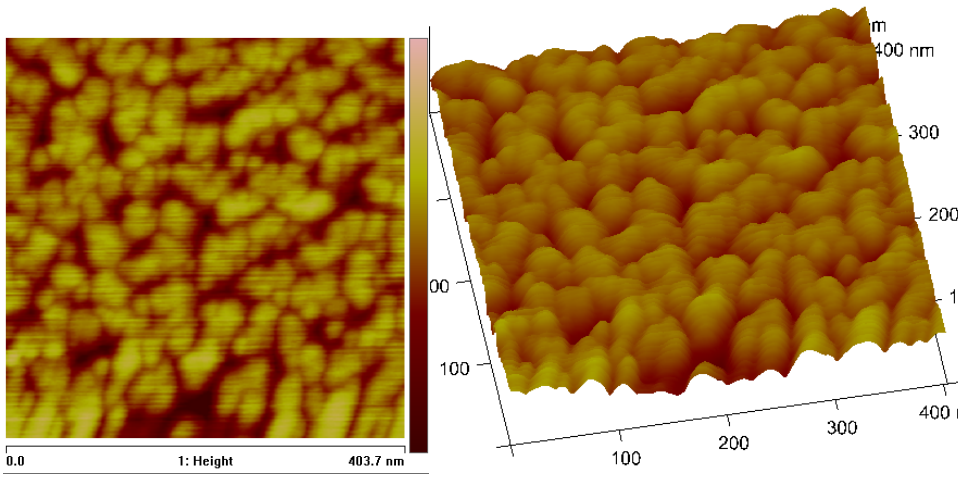


Figure 20 AFM image of 50 cycle HfO_2 on graphene with evaporated Al seed layer.

However, the oxide deposited in this method suffers from trap charges and defects that degrades the tunneling characteristics and hence poor modulation of the collector current of the GHET.

Beside their thickness, these dielectrics have relatively large conduction band offsets with graphene (3.3 eV for Al_2O_3 and 2 eV for HfO_2), which cause a dramatic decrease of the current tunneling probability through the barrier and, thus, α_{BC} becomes very poor. Alternatively, one can use a semiconductor instead of an oxide dielectric as the base-collector barrier. Since the semiconductors can typically form a smaller band offset with graphene compared to oxides (for example, ~0.3eV for n-Si[47], ~0.5 eV for Ge, ~0.7eV for GaN**[72]**), they have a strong band bending effect at the Schottky junction with a metal, which can provide a steep triangular barrier. Therefore, the required field to achieve a given tunnel barrier width is much lower than for insulators as shown in Figure 21. The doping

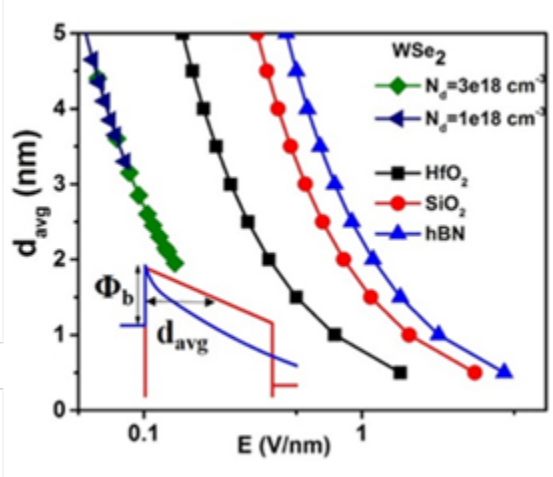


Figure 21 Average tunneling distance in graphene/Oxide and graphene/semiconductor junctions as a function of thickness.

density and the barrier thickness are additional parameters that can be tuned in semiconductor-based barriers to further improve α_{BC}. Figure 22 shows the energy band diagram of the proposed HET structure with the graphene/semiconductor heterojunction as

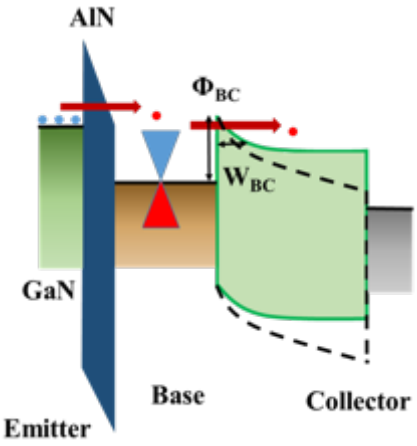


Figure 22 Energy band diagram of the proposed GHET with graphene/semiconductor as the base-collector junction.

the base-collector barrier. The effective tunnel barrier width (W_{BC}) at non-positive V_{CB}(solid line) is large enough to block the tunneling of carriers from the base to collector, similar to a conventional metal/semiconductor heterojunction. In the reverse bias condition ($V_{BC} > 0$ V), the tunnel barrier width is reduced (dotted lines), therefore the carrier tunneling probability would increase. However, the deposition of conventional semiconductors on graphene encounters the same challenges as the oxides, which is non-uniformity and poor material quality. In this project, we overcame this difficulty by using layered semiconductors from the family of transition metal dichalcogenides (WSe_2, MoS_2, SnS_2 etc.). Thin-films of these materials, as thin as a monolayer, can be easily obtained by mechanical exfoliation owing to weak interlayer van der Waals forces. The atomic layers

can then be mechanically transferred on any arbitrary substrate or paired with another atomic layer to form a van der Waals heterojunction with a defect-free, sharp interface.

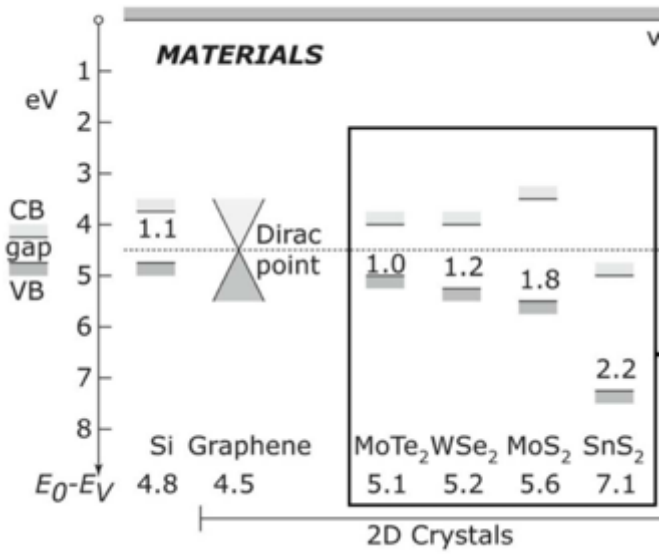


Figure 23 Energy band alignment of various common 2D semiconductors with respect to graphene (adapted from [73])

1.3 Challenges of graphene/semiconductor van der Waals heterostructure

Although there are many layered 2D semiconductor, most of these materials have not been well studied for vertical transport or to form van der Waals heterostructures with other materials. In addition, the large area growth of 2D materials has been mostly limited to graphene and monolayer MoS_2, while the growth for other materials is still in the early stage. As a result, micromechanically exfoliated materials from bulk crystals remain the major materials source. These crystals usually have variation in materials properties when collected from different sources. As a result, before integrating van der

Waals heterostructure into graphene-on-GaN HET, these 2D materials and their heterostructures have to be studied properly with a reliable heterostructure fabrication technique.

2 VERTICAL TRANSPORT IN VAN DER WAALS HETEROSTRUCTURES

Two-dimensional crystals based on atomically thin-films of layered semiconductors, such as the family of transition metal dichalcogenides (TMDCs), offer an attractive platform for various optoelectronic applications [74-87] that stems from their unique electrical, mechanical, and optical properties. The 2D crystals derived from layered crystals, such as graphene, molybdenum disulfide (MoS_2), and hexagonal boron nitride (h-BN), have no dangling bonds on their surfaces. This is in distinct contrast to their counterpart quasi low-dimensional semiconductors, which are produced by thinning down conventional 3D crystals. The trapping sites induced by the dangling bonds in 3D crystal-derived quasi low-dimensional semiconductors are considered to be a major problem as they become trap and recombination sites. 2D electronics can take advantage of the absence of dangling bonds to provide high quality electronic devices on an atomic scale.

The unique optoelectronic and crystal properties of atomically thin 2D crystals make them particularly attractive for heterojunction devices, which can potentially overcome some of the problems that conventional heterostructure devices face and thin 2D crystals also demonstrate novel photovoltaics and optoelectronic applications. Lee *et al* [81] reported an atomically thin p-n vertical junction consisting of van der Waals-bonded monolayers of MoS_2 and WSe_2. The junction shows strong rectifying electrical characteristics and photovoltaic response. Additionally, Fang *et al*.[88] demonstrated evidence of strong electronic coupling between the 2D MoS_2 and WSe_2 layers, which leads to a new photoluminescence (PL) mode in this artificial van der Waals heterostructure.

A very promising field of applications for van der Waals heterostructures of 2D crystals is as interband tunneling transistors for low power applications. Such van der Waals

heterostructures can, in principle, benefit from atomically sharp interfaces. This is crucial for tunneling devices that suffer from impurities and interfacial defects. Moreover, the wide range of available 2D crystals allow different band-edge alignments with distinct band energy structures, ranging from the gapless graphene with a symmetric electron and hole band structure to the wide band gap semiconductors and insulators.

Several in-plane tunneling transistors based on 2D and 1D semiconductors, such as carbon nanotubes[89], bilayer graphene[90], graphene nanoribbons[91], and so forth, have been studied. However, interlayer tunneling devices, which require tunneling in the vertical direction of 2D crystals, are still in their early stages and need further in-depth studies to obtain band structure parameters and tunneling probability along their out-of-plane direction to assess their suitability for high performance tunneling transistors. Nevertheless, some vertical field-effect transistors (FETs) comprising stacks of 2D crystals have already been reported. Britnell *et al*.[46] demonstrated graphene/h-BN/graphene vertical tunneling transistors with few-layer h-BN as the tunneling barrier. This device shows quantum electron tunneling through the barrier modulated by electrostatic gating of the graphene layers.

Recently, Yan *et al*. [92] demonstrated an Esaki diode based on a heterojunction composed of a van der Waals stack of $SnSe_2$ and black phosphorus crystals separated by a native thin tunneling barrier. Their diode showed strong negative differential resistance (NDR), which confirms band-to-band tunneling in this van der Waals heterojunction. However, black phosphorus is unstable when exposed to ambient conditions and rapidly degrades[93]. As mentioned above, 2D crystals that have stable chemical structures, such as MoS_2 and WSe_2, are very promising for creating ultra-clean, defect-free heterointerfaces. In a pioneering

work, Roy *et al*. [94] reported evidence of band-to-band tunneling in a MoS_2/WSe_2 diode. Esaki diode characteristics were observed with NDR at temperatures below 125 K. The authors speculate that band-to-band tunneling occurs in the vertical direction. However, artificially stacked micromechanically exfoliated flakes of different 2D semiconductors have been used in all of these works as the heterostructure growth technology in the early stage.

To integrate graphene/semiconductor van der Waals heterostructure in HETs, we need to overcome two challenges, i) to develop a fabrication technology that ensures clean interface for quantum mechanical tunnelling and ii) to understand the out-of-plane transport through these 2D semiconductors and their heterostructures . Although there are a large number semiconducting 2D materials, only few of them are stable in ambient environment. We choose two of the most stables 2D semiconductors, MoS_2 and WSe_2, as the potential candidate to integrate in graphene-on-GaN HET. To develop understanding of these two materials, we studied their transport properties in both in-plane (chapter 4) and out-of-plane (this chapter).

Despite the earlier work on the optoelectronic properties of MoS_2/WSe_2 devices, the transfer characteristic features of such devices are yet to be fully discussed in the literature. The first part of this work studies a novel feature in the transfer characteristics (I_d–V_g) and transconductance (g_m) of a generic MoS_2/WSe_2 hetero-FET. We present an optimized device geometry to enhance the transfer characteristic parameters to be suitable for high performance electronics. We then discuss the possibility of band-to-band tunneling in this heterojunction. We answer the question whether the vertical (or out-of-plane) direction is the dominant path for band-to-band tunneling in the MoS_2/WSe_2 heterojunction by

simulating and comparing the band diagrams of the heterojunction in both the in-plane and out-of-plane directions. We also design a MoS_2/WSe_2 tunnel diode based on the information obtained from the simulation and we investigate its tunnel diode characteristics. Finally, a novel application of the optimized MoS_2/WSe_2 hetero-FET as a building block for multi-valued logic is provided.

2.1 Fabrication flow for van der Waals heterostructure devices

In a typical two-dimensional materials devices, the gate efficiency (dE_F/dV_g) is very low, due to the very thick gate oxide (300 nm SiO_2) used in the device. Therefore, very large gate voltages are required to operate the transistors. To date, 2D devices have mainly been limited to either single top-gated transistor or single back-gated transistor configurations with Si substrates acting as a global back gate, which are normally coated with a very thick SiO_2 layer as the dielectric. The reasons for using such a thick oxide are twofold: to obtain sufficient optical contrast to locate micrometre-wide flakes, and to avoid large gate leakage, because the Si substrate is a global back gate with 100% overlap with the S/D (source/drain) contacts and the measurement pads.

To enhance the performance of the transistors and improve the gate efficiency, we need to increase the gate dielectric capacitance, whilst keeping the gate leakage current as low as possible. Herein, a simple solution is used to solve this problem: we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using the thick SiO_2 layer. In this configuration, the transistor benefits from a global back gate that provides lower contact resistance, and the gate leakage current is also reasonably low.

For the scaled gate dielectric devices, 30 μm × 30 μm via holes are defined on a 90 nm SiO_2/Si substrate with electron-beam lithography. These via holes are then wet etched followed by an atomic layer deposition of 10 nm HfO_2 using tetrakis (dimethylamido)-hafnium (IV) and water at 250 °C. The sample is then annealed in forming gas at 400 °C to reduce the bulk oxide traps. The subsequent lithography steps are the same as in regular devices.

Figure 24 shows a representative hetero-FET comprising MoS_2 and WSe_2 thin films contacted with Au and Pt lines. Measurement pads (not shown) and wide connecting lines are kept on a thick SiO_2 plateau and lines lying on the bottom of the SiO_2 via are kept below 400 nm in width to maintain a low gate leakage current.

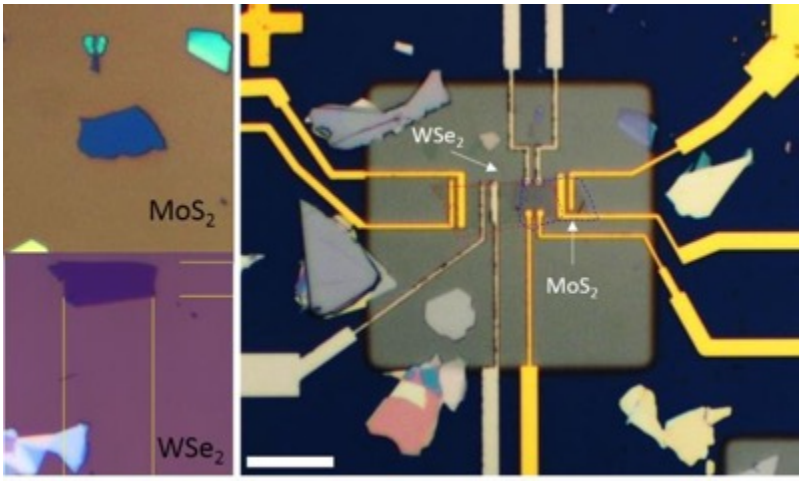


Figure 24: Optical images of representative exfoliated MoS2 and WSe2 flakes as well as the final MoS2/WSe2 hetero-FET fabricated in a 90 nm deep SiO2 via coated with 10 nm HfO2. Flakes are contacted with Au and Pd. The scale bar is 10 μm.

The transistor structure used in this work shows an average gate-leakage current $|I_{gate}|<100$ pA/μm in the measurement range, compared with $|I_{gate}|<1$ pA/μm for the device with 300 nm SiO_2, effective oxide thickness (EOT) =300 nm. Figure 25 shows the capacitance–voltage (C–V) characteristics of a generic multilayer MoS_2 capacitor with an Au electrode and Si substrate as the capacitor electrode and 10 nm HfO_2/native SiO_2 as the dielectric. The capacitor shows a clear transition from depletion to accumulation modes with EOT=3.3 nm. Heating the device to 360 °C in a H_2/Ar atmosphere resulted in sharper C–V curves owing to annealing of the MoS_2/HfO_2 interfacial defects.

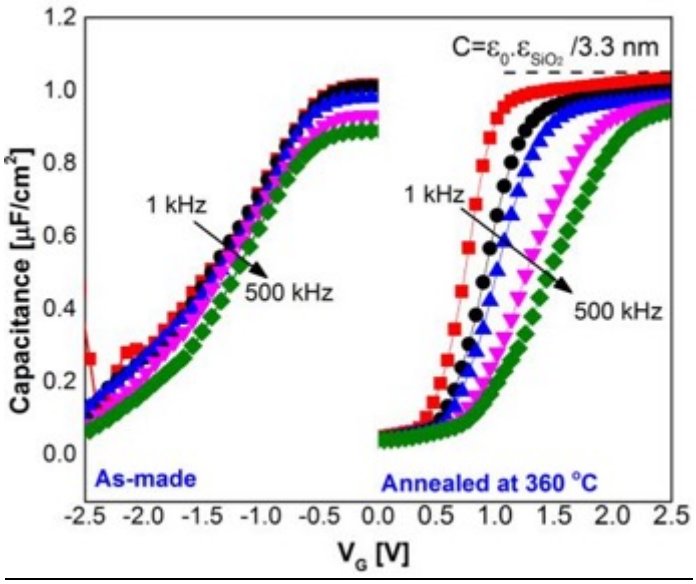


Figure 25 As-made and after-annealing capacitance–voltage characteristics of a multilayer MoS_2 capacitor at different frequencies in the 1 to 500 kHz range.

Figure 26 (a) shows the schematic of a MoS_2-FET that was built in 90-nm-deep SiO_2. The transfer characteristics of a monolayer and a 4-layer MoS_2-FET are compared in Figure 26(b). The monolayer MoS_2 device shows a minimum sub-threshold swing (SS_{min}) of 71 mV/dec, while the multilayer device shows a SS_{min} of 105 mV/dec (Figure 26(c)). Here,

$SS = (\frac{d(\log 10 I_d}{dV_g})^{-1} \approx \ln\frac{kT}{q}(1+\frac{qD_{it}}{C_{ox}})$, where k is the Boltzmann constant, C_{ox} is the gate dielectric capacitance and D_{it} is the trap charge density at the dielectric/channel interface. For D_{it}=0, SS=60 mV/dec at room temperature, which is the thermionic limit of SS in conventional MOSFETs. The deviation of SS from 60 mV/dec in the monolayer MoS_2-FET can be attributed to the presence of trap charge density in the MoS_2/HfO_2 interface and the even larger SS in the multi-layer MoS_2-FET is further affected by the large inter-layer resistance and larger channel body in the multi-layer MoS_2 that lowers the electrostatic control of the gate over the channel. Figure 26 (d) shows the I_d–V_g plot of a parallel-mode MoS_2/WSe_2 hetero-FET. In contrast to the in-series mode (Figure 26 (c)), in the parallel mode, both source and drain electrodes are in contact with the overlapping MoS_2/WSe_2 region, forming a parallel bilayer FET's channel. In this configuration, the I_d–V_g curve resembles the sum of the I_d–V_g of two isolated MoS_2 and WSe_2 FETs. As depicted in Figure 26 (d), I_d–V_g has two almost symmetric electron and hole conduction branches with a narrow OFF-state region with I_{ON}/I_{OFF} in excess of 10^5 and SS_{min} of 110 mV/dec. In this configuration, at large positive V_g values, both MoS_2 and WSe_2 are in the electron accumulated mode and the channel is *n*-type. At large negative V_g values, the conduction is dominated by the *p*-type conduction of the WSe_2 component in the channel, while the MoS_2 sub-channel is depleted.

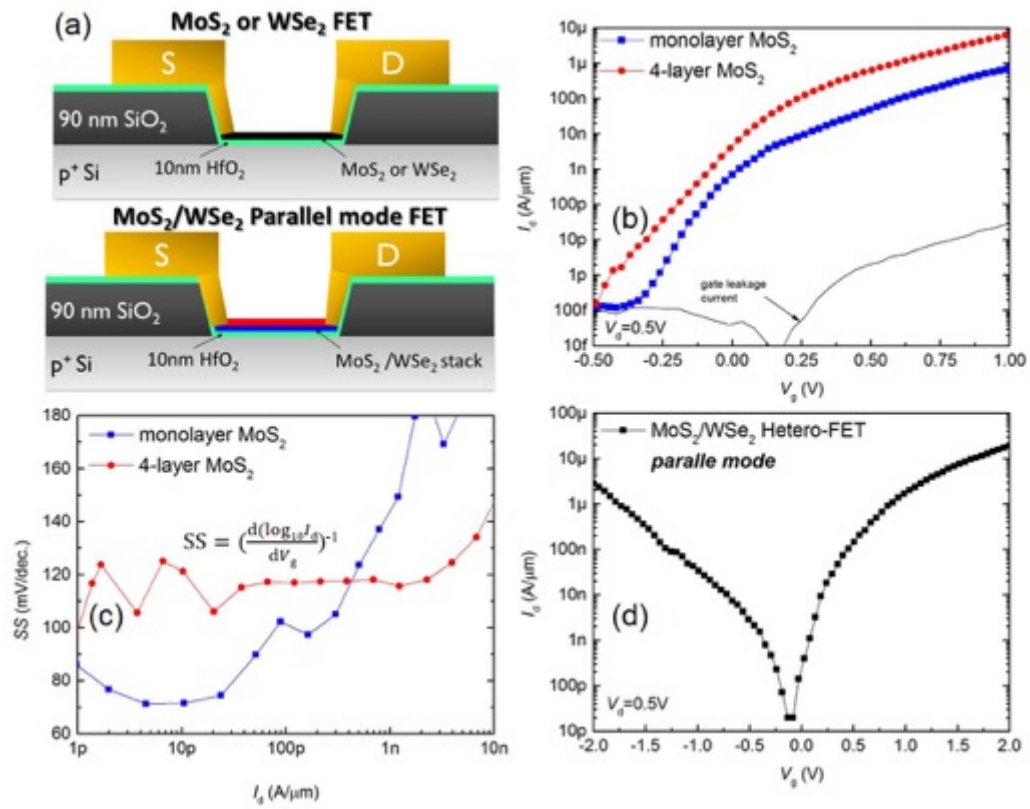


Figure 26 (a) Schematic of a generic MoS_2 or WSe_2 FET and a MoS_2/WSe_2 hetero-FET in parallel mode using a thin HfO_2 gate dielectric with SiO_2 contact isolation. (b) I_d–V_g of the monolayer and 4-layer MoS_2-FETs. (c) Sub-threshold swing (SS) of the device shown in (b). (d) I_d–V_g of a representative MoS_2/WSe_2 hetero-FET. Here, the drain current I_d in (b) and (d) is plotted along the vertical axis and in (c) along the horizontal axis on a log scale.

2.2 **Transport characteristics of type-II heterojunction tunnel diode**

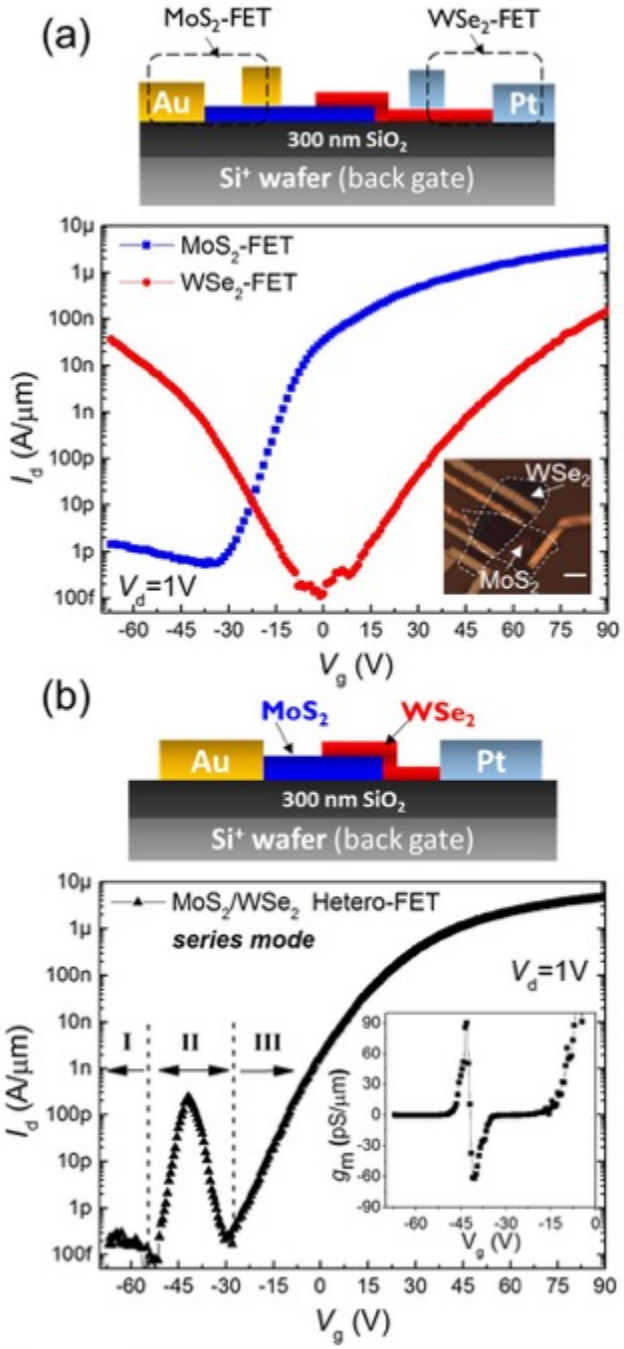


Figure 27 (a) Transfer characteristics (Id–Vg) of a back-gated few-layer MoS_2- and WSe_2-FET. The inset shows an optical image of a typically stacked MoS_2/WSe_2 FET. The scale bar is m. (b) I_d–V_g of the MoS_2/WSe_2 heterojunction FET in the series measurement mode. The inset shows the transconductance centered around the peak in region II. The schematics show the corresponding device measurement setups.

Figure 27 (a) shows the transfer characteristics (I_d–V_g) of generic few-layer (2–4 layers, confirmed by atomic force microscopy (AFM)) MoS_2- and WSe_2-FETs, where V_g is the voltage applied to the substrate. The MoS_2 FET, consistent with previous literature, is shown to be an *n*-type semiconductor, while WSe_2 demonstrates both *n*- and *p*-type characteristics giving rise to ambipolar transfer characteristics with a relatively wide OFF-state region. The symmetry of the electron and hole conductions of the WSe_2 FETs can be strongly affected by the Schottky barrier at the WSe_2–metal junction. High performance ambipolar WSe_2-FETs have already been reported using dissimilar low and high work function metal contacts to obtain low-resistance, ohmic contacts to electrons and holes, respectively [80, 95].

Figure 27 (b) plots the transfer characteristics of a MoS_2/WSe_2 hetero-FET arranged in the in-series mode. In this configuration, the MoS_2 and WSe_2 films form an overlapped region so that the source and drain electrodes (S/D) are in contact with the films, whilst leaving the overlapped region away from direct contact with the electrodes. In this configuration, electrons injected from the source to the MoS_2 film have to proceed through the WSe_2 film in the overlapped region and continue to the drain electrode. Therefore, the MoS_2 and WSe_2 films can independently modulate the overall transport characteristics of the FET. As shown in Figure 27 (b), I_d–V_g, of a back-gated in-series MoS_2/WSe_2 FET shows three distinct regions. In region I (V_g<–53 V), I_d is very low, within the noise of the measurement setup. This region is modelled by an *i*-p^+ junction because the MoS_2 is depleted, while the WSe_2 shows hole accumulation. Therefore, the electron path from source to drain is blocked by highly resistive depleted-MoS_2, which results in low current. However, in region II (–53 V<V_g<–30 V), the current increases and shows a peak with

substantial current centred at −42 V with a peak-to-valley ratio in excess of 1000. This region corresponds to the condition where the MoS_2- and WSe_2-FET are both in their sub-threshold regimes, where decreasing V_G from −30 V to −53 V leads to an exponential increase of hole conduction on the WSe_2 side and an exponential decrease of the electron concentration on the MoS_2 side toward its depletion regime. Hence, this condition can be assigned to a p^--n^- junction. The resulting current peak shows a rapid change in the gated transconductance ($g_m=dI_d/dV_g$) from positive to negative, as shown in the inset of Figure 27(b). This feature, which occurs when one of the semiconductor layers (MoS_2 here) is near its depletion condition, is distinct from the negative transconductance owing to the resonance tunneling phenomena, which occurs at matched carrier densities in two-dimensional electron gas systems (2DEGs) [96-99]. We will then further discuss this sign-changing g_m characteristic and its possible application.

At larger V_g, region III, the current increases in the MoS_2 monotonically with increasing V_g. The current in this region is dominated by electron conduction in both the MoS_2 and WSe_2 regions, as both are in their electron accumulation regimes. Therefore, for this region, the system can be modelled by an *n*-*n* heterostructure.

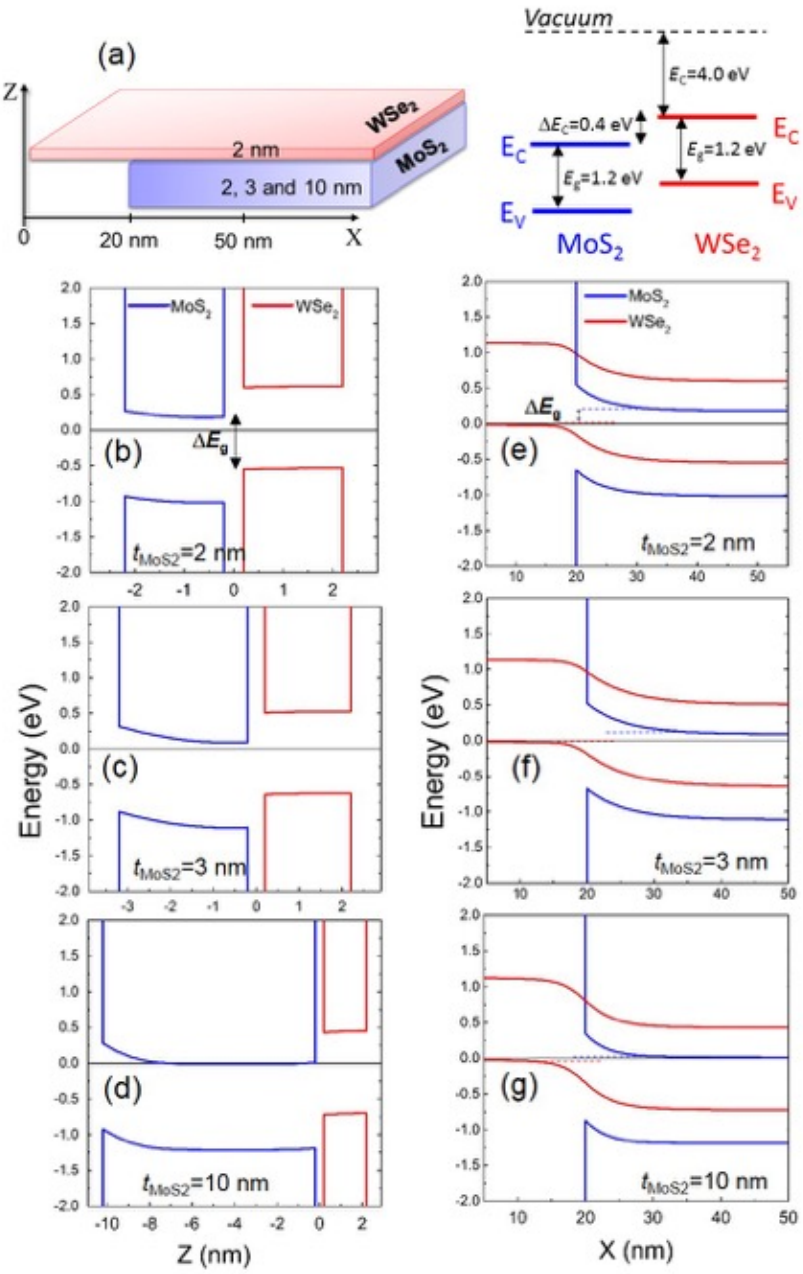


Figure 28: (a) Schematic of a MoS_2/WSe_2 heterostructure and the conduction band (EC) and valence band (EV) positions that are used for calculation of the band diagrams. (b–d) Calculated band diagrams of MoS_2/ WSe_2 heterojunctions in the out-of-plane direction at the middle of the overlapped region (X=50 nm). The WSe_2 is 2 nm thick while the thickness of MoS2 varies as (b) 2, (c) 3 and (d) 10 nm. (e–g) In-plane band diagram of the same heterojunctions along the X-axis of the schematic in (a), at edges of the MoS_2 and WSe_2 films. In all the structures, the WSe_2 charge is $5\times10^{18}/cm^3$ and the MoS_2 charge density is $1\times10^{19}/cm^3$ and the gap between the MoS_2 and WSe_2 films is 4 Å, assuming that there is a van der Waals gap between the two films.

2.3 Band to band tunnelling in MoS_2/WSe_2 heterojunction diode

Similar to 2DEG bilayer heterostructures [90, 100], the most interesting transport regime in the MoS_2/WSe_2 FET shown in this work is when the MoS_2 and WSe_2 layers are oppositely charged and form a *p-n* heterojunction. Heterostructure semiconductors are widely used for the fabrication of tunneling FETs (TFETs), which are among the most promising devices for achieving very low power operation, owing to the possibility of achieving a steep inverse sub-threshold slope below the thermionic limit of 60 mV/decade. In principle, heterojunction TFETs, using two different semiconductors forming a vertical or horizontal junction, are interesting compared with homojunction TFETs, as they enable bandgap engineering to form a heterojunction with a narrower effective bandgap, which improves the tunneling probability and, thus, the drive-current which significantly depends on the bandgap. A variety of semiconductor heterostructures, especially those based on III–V compounds, have already been fabricated to make heterojunctions with the desired bandgap features. Examples include GaAsSb/InGaAs[101, 102], InP/InGaAs[103] and GaSb/InAs[104]. Analogous to these conventional bilayer heterojunctions, bilayer heterojunctions of van der Waals stacked 2D materials, such as the ones studied in this work, are considered very promising for tunneling devices. As was mentioned earlier, the charge transferred between the layers can strongly modulate the energy bands of WSe_2 and MoS_2 forming a region with an abrupt, atomically precise interface that is of high importance, as non-idealities, such as defects and non-abrupt band-edges, owing to, for example, the random doping distribution case, are critical in TFET technology.

To determine the possible band-to-band tunneling paths in a MoS_2/WSe_2 heterojunction, we calculated the band diagram of some representative MoS_2/WSe_2 heterojunctions with different charge densities and film thicknesses. The details of the calculations can be found later in this chapter. Figure 28(b–g) show band diagrams of the heterojunction between a 2-nm thick p-doped WSe_2 (equivalent to a three-layer WSe_2) with charge density of $5\times10^{18}/cm^3$ and an n-doped MoS_2 with bulk charge density of $1\times10^{19}/cm^3$ for three different thicknesses, i: t_{MoS2}=2 nm, t_{WSe2}=2 nm , ii: t_{MoS2}=3 nm, t_{WSe2}=2 nm, iii: t_{MoS2}=10 nm, t_{WSe2}=2 nm (Figure 28 (a) shows a schematic of the MoS_2/WSe_2 layers and the conduction band and valance band alignments used for calculation of the band diagrams). The band diagram in the transverse direction (i.e. Z) (Figure 28 (b–d)) of the heterojunction interface shows a minimum effective band gap of ΔE_g= 0.85 eV between the conduction band of WSe_2, $E_{C,WSe2}$ and the valance band of MoS_2, $E_{V,MoS2}$, which corresponds to t_{MoS2}=10 nm, t_{WSe2}=2 nm. This is a relatively large band gap for a tunneling device compared with other proposed heterostructures that have been developed for high performance TFETs, since the tunneling probability decreases as the effective band gap increases. In addition, the weak van der Waals interaction between the layers, owing to the random orientation of their lattices, leads to an effective vacuum potential barrier. This further suppresses the tunneling probability and therefore the tunneling current. Therefore, vertical tunneling in MoS_2/WSe_2 seems very unlikely. However, the band diagram along the horizontal direction (i.e. X), plotted in Figure 28(e–g) shows promising features. In fact, owing to the thin nature of the films, the interaction between layers at the junction leads to substantial band bending between the overlapped and non-overlapped regions. As expected, the band bending is stronger in the thinner film and the effective band gap ΔE_g strongly decreases with

increasing the asymmetry of the thicknesses of the layers. In the case of 2 nm WSe_2/10 nm MoS_2, a small in-plane $\Delta E_g < 50$ meV is achieved, compared with 0.85 eV in the transverse band diagram at the overlapped region. The band diagram of the 2 nm WSe_2/10 nm MoS_2 heterojunction predicts the occurrence of NDR owing to band-to-band tunneling between the conduction band (E_c) of MoS_2 in the overlapped region and the valance band (E_v) of WSe_2 of the non-overlapped region.

Before discussing the experimental results of the predicted tunneling performance, we would like to highlight once again that in modeling 2D materials-based heterojunctions, in addition to the band alignment in the transverse direction, the band structure modulation along the interface needs to be taken into account to obtain a comprehensive evaluation of the transport in any ultra-thin, low or moderately doped heterostructure device. This also enables the selection of suitable materials for NDR enhancement. Additionally, despite the promising features of van der Waals TMDC heterostructures, the out-of-plane carriers possess heavier masses in the layered materials than the masses parallel to the layers (e.g., MoS_2: in-plane mass=0.45 m_e, out-of-plane mass=1.73 m_e[105]). Additionally, the out-of-plane resistance can be orders of magnitude larger than the in-plane resistance, which is a consequence of their anisotropic nature owing to the weak van de Waals interlayer interaction compared with the strong covalent in-plane interaction between atoms. However, a comprehensive, quantitative study is required to obtain an in-depth understanding of tunneling transport in both the in-plane and out-of-plane directions in 2D heterojunctions. Nevertheless, knowing that, in general, the tunneling transmission probability[90, 106] is $T(F) = \exp\left(\frac{-\pi (m^*_{tunnel})^{\frac{1}{2}} \Delta E_g^{\frac{3}{2}}}{2\sqrt{2}\hbar q F}\right)$ (where m^*_{tunnel} is the carrier effective mass in the tunneling direction, ΔE_g is the effective bandgap and F is the electric

field across the semiconductor body), we can anticipate that the heavier carriers in the out-of-plane direction as well as the larger band gap can dramatically decrease the tunneling probability in this direction compared with the in-plane direction. Hence, given the smaller in-plane carrier masses and band gap, the in-plane heterojunction of TMDC atomic layers, as discussed above, promises to be a practical structure for actual tunneling devices.

Next, to evaluate the possibility of band-to-band tunneling in an in-plane MoS_2/WSe_2 heterojunction, as suggested by the afore-discussed band diagram, we study a transistor whose channel comprises of a thickness-asymmetric ~2 nm WSe_2/~10 nm MoS_2 stack (thicknesses confirmed by AFM measurements). To enhance the performance of the transistors and improve the gate efficiency, we need to increase the gate dielectric capacitance and yet keep the gate leakage current as low as possible. Herein, we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using a thick SiO_2 layer to optimize the trade-off between the gate efficiency and gate-source/drain leakage current.

Figure 29 (a) shows the room temperature I_d–V_d in reverse and forward bias regions at different V_g values. In the forward bias region, a clear NDR with a maximum peak to valley of 1.6 is observed at V_g=0.15 V. The insets show the NDR region in the linear scale for V_g=0.15 and 0.60 V and the NDR peak to valley ratio versus V_g, which decreases monotonically by increasing V_g to 0.60 V. In fact, applying a more positive V_g widens the gap by lowering the energy of the bands, which makes the NDR process more difficult and explains the decrease of the peak-to-valley values toward zero. Schematic band diagrams of the in-plane MoS_2/WSe_2 junction at different bias regimes are shown in Figure 29(b).

Figure 29 (c) shows the conductance ($G = \frac{I}{V}$) for V_g=0.15V. Our gated tunneling diode, in the reverse bias regime, shows an average slope of $S = 75$ mV/dec over two orders of conductance magnitude, and a maximum curvature coefficient of $\gamma_{max} = 62.2\ V^{-1}$ above the noise level, at V_d=–0.45 V.

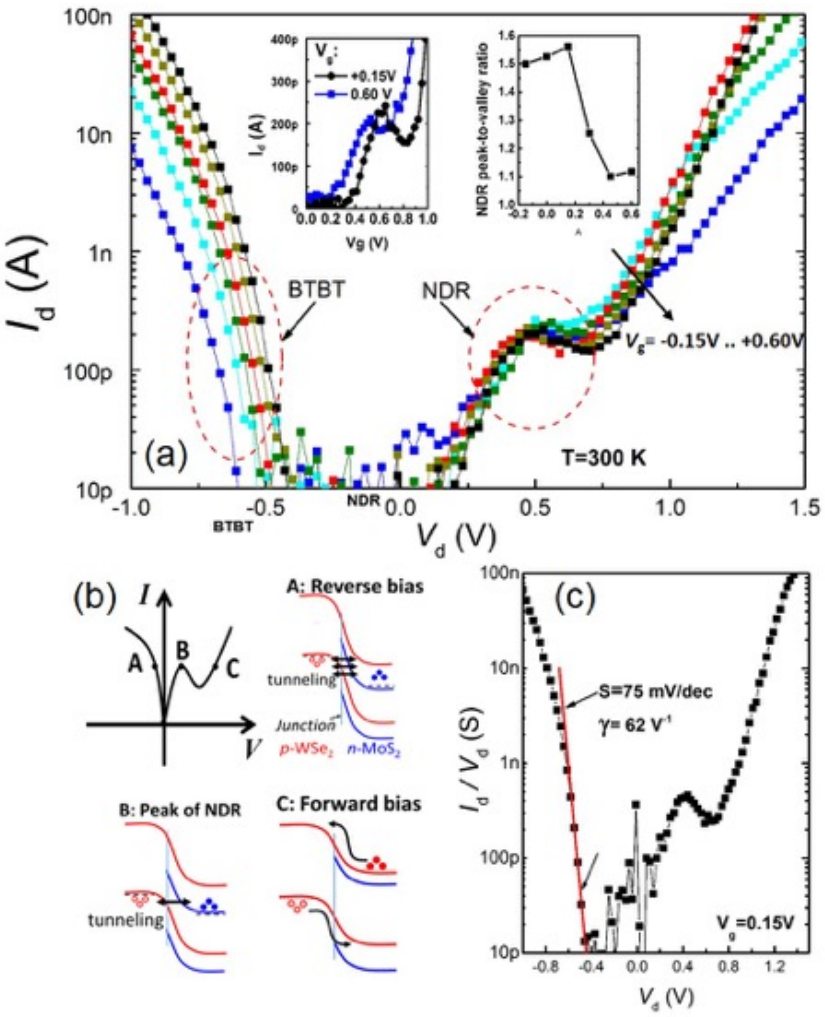


Figure 29: (a) Room temperature I_d–V_d of a 10 nm MoS_2/2 nm WSe_2 transistor at different Vg values. The insets show I_d–V_d at the NDR region with a linear scale for V_g= +0.15V (black) and +0.60 V (blue) on the left and NDR peak-to-valley ratio versus V_g on the right. (b) Schematic band diagrams of a MoS_2/WSe_2 junction at points A,B, and C illustrating the three different bias regimes. (c) Conductance ($G=I_d/V_d$) versus V_d at V_g=0.15 V.

The curvature coefficient is an important figure of merit parameter for designing high-performance tunneling diodes which are promising devices for several applications, such as high frequency detectors[107]. Because the operation of these diodes is based on band-to-band tunneling, their *I-V* curvature characteristics are not limited by their thermionic emission of carriers. Our tunnel diode reached the typical goal of $\gamma > 40\ V^{-1}$ for backward diode operation [108]. The best γ reported so far, based on Si and III–V semiconductor-based backward diodes, are in the range of 47 to 70 V^{-1} in the low V_d regime [109-111], which places our MoS_2/WSe_2 tunnel diode among the highest performance tunnel diodes reported to date. However, to obtain a transistor with a sub-threshold slope SS<60 mV/dec, γ should be larger than 80 V^{-1} [107]. Given the fact that unlike the conventional semiconductor devices, where the charge concentration of the semiconductor is well-controlled by doping techniques, in this MoS_2/WSe_2 device, its unintentional, natural doping is not prepared through any specific doping approach. Developing efficient doping approaches to precisely control the charge density in 2D crystals and yet preserve their excellent properties will certainly aid in the preparation of the sharp band-edge feature in the 2D heterojunctions that is needed to observe the sharp threshold characteristics beyond the SS=60 mV/dec limit.

2.4 First demonstration of ternary logic inverter using van der Waals heterostructure

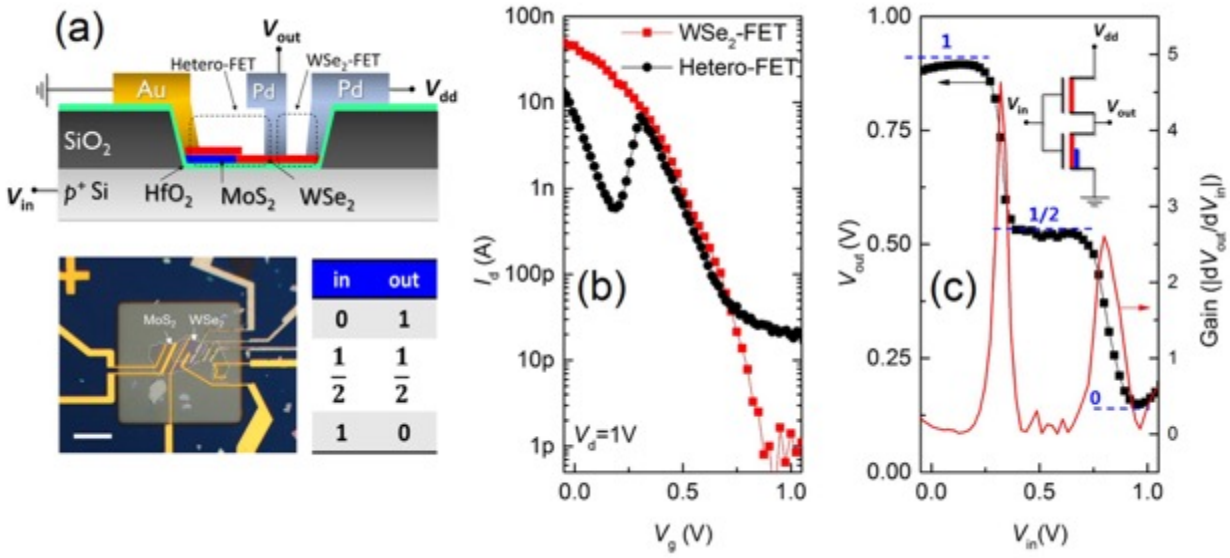


Figure 30: (a) Schematic of the ternary inverter, an optical image of the device, and an input–output table of the inverter. (b) Comparison of I_d–V_g curves of the hetero-FET and WSe_2-FET shown in (a). (c) V_{out} versus V_{in} plot of the ternary inverter showing three distinct levels of logic. The inset shows a circuit schematic of the inverter.

Negative transconductance has been demonstrated in gated resonant tunneling devices [96] as well as modulation doped FETs [98]. Among different applications of negative transconductance, multi-valued logic (MVL) [97] has attracted much attention. Owing to a higher number of logic states, MVL has the potential for higher data storage in less area as compared with binary logic.

In the past decades, MVL, such as ternary (three-level logic), has been considered as an alternative to binary logic and, so far, significant development has been achieved in the theory and design of ternary-based arithmetic operations [112]. Different MVL architectures, such as current-mode [113] and voltage-mode [114] multi-valued CMOS, as well as multi-valued charge-coupled devices [115] have already been demonstrated.

Herein, we demonstrate the application of MoS_2/WSe_2 heterojunction FETs with the sign-changing transconductance feature for a ternary inverter using only one type of FET (p-FET). The inverter, as schematically depicted in Figure 30(a), comprises two FETs built on a WSe_2 film partially stacked on a MoS_2 film. The WSe_2 end is contacted by Pd and the overlapping region is contacted with Au. This configuration can be considered as a WSe_2-FET in series with a parallel-mode MoS_2/WSe_2 FET. For this device, an asymmetrical stack of a few-layer WSe_2 and a multilayer MoS_2 were used. The work function difference of MoS_2 and WSe_2[116] leads to charge accumulation of electrons in MoS_2 and of holes in WSe_2. Given the thin body of the WSe_2, this charge transfer creates two distinct regions in WSe_2: a part that overlaps with the MoS_2 and a non-overlapped region that can be considered as p^+-p^- regions. This multi charge density profile induces multi-threshold voltages (multi-V_{th}) in the transfer characteristics of a FET comprising the p^+-p^- regions. Figure 30(b) compares the I_d–V_g curves of the WSe_2-FET built on the overlapped region with the curve of the combined WSe_2 and overlapping WSe_2/MoS_2 (p^+-p^- channel), which is analogous with the FETs in Figure 27, and which we named a parallel-series mode FET. In region I of the I_d–V_g curves, which corresponds to the threshold regime, a strong decrease of the current, which gives rise to the negative transconductance feature, is observed. As a result, the current of the parallel-series FET in this region is lower than its WSe_2 counterpart FET, which shows regular I_d–V_g behaviour. In region II, corresponding to the sub-threshold region of both FETs, both devices behave similarly with parallel I_d–V_g curves. However, in region III or the OFF-state region, the WSe_2-FET has substantially lower current than the parallel-series FET owing to the fact that the OFF current of the parallel-series FET is larger. In the inverter configuration (inset of Figure 30(c)), the back gate is used for the

input voltage (V_{in}), the middle electrode for output voltage (V_{out}) and the sides electrodes for the source and supply voltage. The three regions described in Figure 30(b), form three distinct levels in the input-output characteristics (V_{out} versus V_{in}) of the inverter, shown in Figure 30(c), corresponding to three logic states. In this plot, V_{in} varies in the range of 0 to 1 V where V_{out} shows a high value of ~0.9 V for $0<V_{in}<0.3$ V, corresponding to state 1, a medium value of V_{out} ~0.5 V for $0.4<V_{in}<0.8$ V, corresponding to state ½, and a low level of V_{out} ~0.15 V for $V_{in}>0.85$ V. The ternary device shown in this work is the first demonstration of how a multi-V_{th} design, enabled by ultra-thin nature of 2D semiconductors and their heterojunction engineering, can be suited and ubiquitous for the design of efficient multi-valued logic circuits.

2.5 van der Waals heterostructure fabrication by dry transfer

The heterojunction devices were prepared by the commonly used pickup and dry transfer methods[1,2]. WSe_2 and MoS_2 are mechanically exfoliated from commercially available bulk crystals using cleanroom grade on a separate pre-cleaned (i.e., Piranha solution, oxygen plasma and solvent cleaning) substrate. A polydimethylsiloxane (PDMS) sheet was cut into small pieces and placed on a pre-cleaned glass slide with double-sided tape. A 6% solution of polypropylene carbonate (PPC, Sigma Aldrich) in chloroform was then spin coated on the glass/tape/PDMS stack. This transfer slide was then loaded into the probe arm of the transfer setup and brought into contact with the desired flake at room temperature. The stage was then heated to 90 °C and maintained at that temperature for 1 min. After the temperature of the stage was returned to room temperature, by natural or forced cooling, the transfer slide was slowly disengaged. This process was repeated for the second flake.

The picked-up heterostructure was transferred to the pre-patterned via holes and heated up to 155 °C to release the polymer. Finally, the polymer was dissolved in chloroform followed by solvent cleaning and annealing (200 sccm Ar/200 sccm H_2) at 360 °C for 3 h.

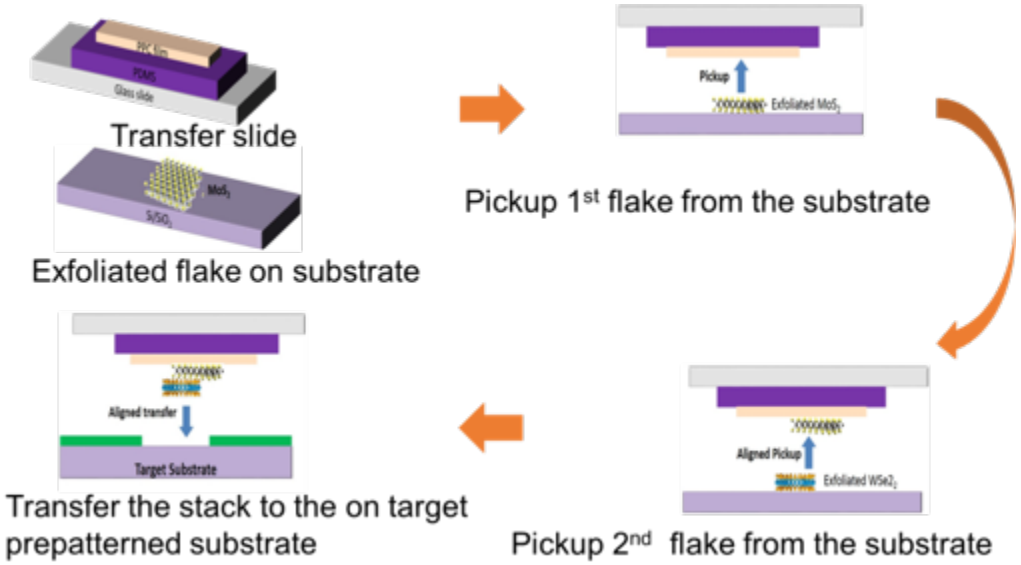


Figure 31**:** Schematic of the heterostructure fabrication by the dry transfer method.

Band diagram calculations

The band diagrams of the MoS_2/WSe_2 heterojunction in this work are obtained using the nextnano semiconductor nanodevice simulation tool[5]. An indirect bandgap of 1.2 eV is used for both MoS_2 and WSe_2 in the simulation, which is consistent with the reported experimental and theoretical bandgap values for few-layer and multilayer values[6]. In-plane masses of $m^*=0.46m_e$ and $m^*=0.33m_e$ are used for MoS_2 and WSe_2, respectively, and the out-of-plane mass of $m^*=1.73m_e$ is used for multilayer films[7,8]. For dielectric constants, in-plane $\varepsilon_r=6$ and $\varepsilon_r=12$ and out-of-plane $\varepsilon_r=4$ and $\varepsilon_r=7$ are used for MoS_2[9,10] and WSe_2[11], respectively. In addition, according to the literature[6], a band offset of 0.4 eV between the conduction bands of multilayer MoS_2 and WSe_2 is included. The weak van der Waals interaction between the layers, owing to the random orientation of their lattices, leads to an

effective vacuum potential barrier. Here, a vacuum barrier of 4 Å is considered in the MoS_2/WSe_2 heterostructure in Figure 32 as the van der Waals gap between the two films.

Figure 32 compares the in-plane and out-of-plane band diagrams of *n*-MoS_2/*p*-WSe_2 heterojunctions with three different combinations of thicknesses, all with the same electron and hole charge densities. The choice of electron and hole concentrations was based on typical values of naturally doped MoS_2 and WSe_2 extracted from their field effect transistors. The conclusion from Figure 32 was that for the given charge densities, a thickness-asymmetric heterostructure is required to achieve a small effective bandgap in the in-plane direction, which can enable band-to-band tunnelling. We compare the impact of different charge densities on the effective bandgap ($\Delta E_g = E_{c,MoS2} - E_{v,WSe2}$) for the best thickness choice in Figure 32, that is, 2 nm WSe_2/10 nm MoS_2. Three different combinations of charge densities were considered. As can be seen, to have a minimum ΔE_g, the hole concentration of WSe_2 (p) needs to be relatively larger than the electron concentration (n) of MoS_2 ($p>n$), while the opposite configuration ($p<n$) results in a relatively large ΔE_g and equal charge densities ($p=n$) shows a small ΔE_g but still larger than the $p>n$ case. As a conclusion, the precise control of the thickness and charge density in the heterostructure components is essential to realize in-plane band-to-band tunnelling; however, regardless of the choice of the thickness or the charge density of the two components, the effective bandgap in the out-of-plane direction remains relatively large (ΔE_g=0.8–0.9 eV) in MoS_2/WSe_2 heterojunctions.

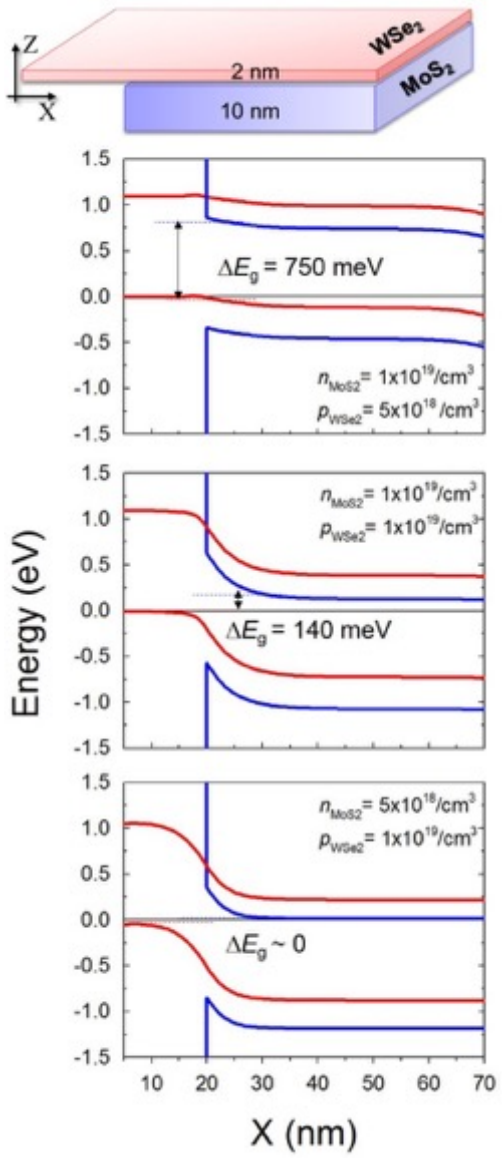


Figure 32: Schematic of a 2 nm WSe_2/10 nm MoS_2 heterojunction and its calculated in-plane band diagrams with three different MoS_2 and WSe_2 charge concentration combinations.

2.6 **Effect of semiconductor thickness on the band to band tunneling**

Figure 33 shows the plots of the I_d–V_d curves of MoS_2/WSe_2 hetero-FETs with different thicknesses, monolayer, few layer (2-4 layers) and multilayer (>4 layers). As is discussed previously, the thickness-asymmetric heterojunctions comprising few layer-WSe_2 and multilayer MoS_2 films are suitable for lateral-tunnelling devices. The representative

devices in Figure 33 show strong NDR. The variation is attributed to sample to sample variation in the natural doping of exfoliated flakes, as well as to imperfections induced by the transferring process. The monolayer MoS_2/few-layer WSe_2 shows diode behaviour with strong rectification, while few-layer/few-layer devices have larger reverse current.

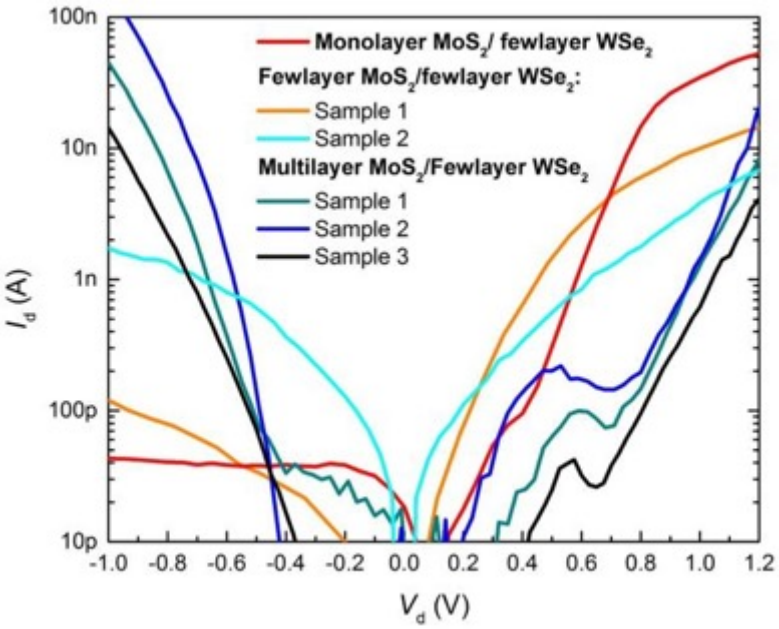


Figure 33: I_d–V_d of several MoS_2/WSe_2 hetero-FETs with different MoS_2 and WSe_2 thicknesses fabricated in this work.

3 GRAPHENE-ON-GAN HOT ELECTRON TRANSISTOR WITH TMD BARRIER

In chapter 1, it was proposed that graphene/semiconductor junction would be an ideal solution for the B-C junction in HET. However, our study in section 4.2 shows that graphene can act as an ohmic contact to MoS_2 which means that graphene/MoS_2 heterostructure will be dominated by the junction leakage. Herein, we propose to use a graphene/WSe_2 base-collector junction, where the graphene-base forms a Schottky barrier to the WSe_2 layer. WSe_2 is an ambipolar semiconductor with a bulk bandgap of 1.2 eV that increases to 1.6 eV in the monolayer. This configuration would potentially benefit from the small graphene/WSe_2 band offset energy (~0.54 eV[117]), which is in the typical range for a graphene/semiconductor junction. The layered nature of WSe_2 enables a thickness control from the monolayer (t ~0.65 nm) to bulk. In this work, we also study the effect of collector layer thickness on the performance metrics of GHET.

Figure 35 presents the schematic of the device structure used in this work. We have used a bulk n-GaN ($N_d \sim 10^{19}$ cm^{-3}) substrate grown by the ammonothermal method to achieve a low threading dislocation defect (TDD) density ($<10^5$ cm^{-2}) emitter. A 3 nm AlN tunneling layer was grown on top by plasma-assisted molecular beam epitaxy. The use of a low TDD density substrate ensures a high film quality and minimal leakage current through the dislocations. A 3 nm GaN layer was used as a capping layer between the AlN and the graphene base.

3.1 MBE growth of high quality AlN tunnel barriers

Samples are grown by MBE in a Veeco Gen 930 system on Ammono bulk GaN substrates. Figure 34 (a) shows the X-ray diffraction (XRD) characteristics of the substrate before the growth. Active N_2 was supplied through a Veeco RF plasma source. All growths were performed in metal-rich regime. The N_2 flux at the substrate position was kept constant at $\sim 2\times10^{-5}$ Torr. The plasma RF power is kept as 200W throughout the growth, corresponding to a growth rate of 105 nm/hr at a substrate temperature of 720 °C. The growth started with a GaN buffer layer with thickness ~180nm. A GaN cap layer is grown after the AlN barrier layer. Figure 34(b) shows the AFM image of the typical GaN/AlN heterostructure after the growth, in which smooth, atomic steps are visible.

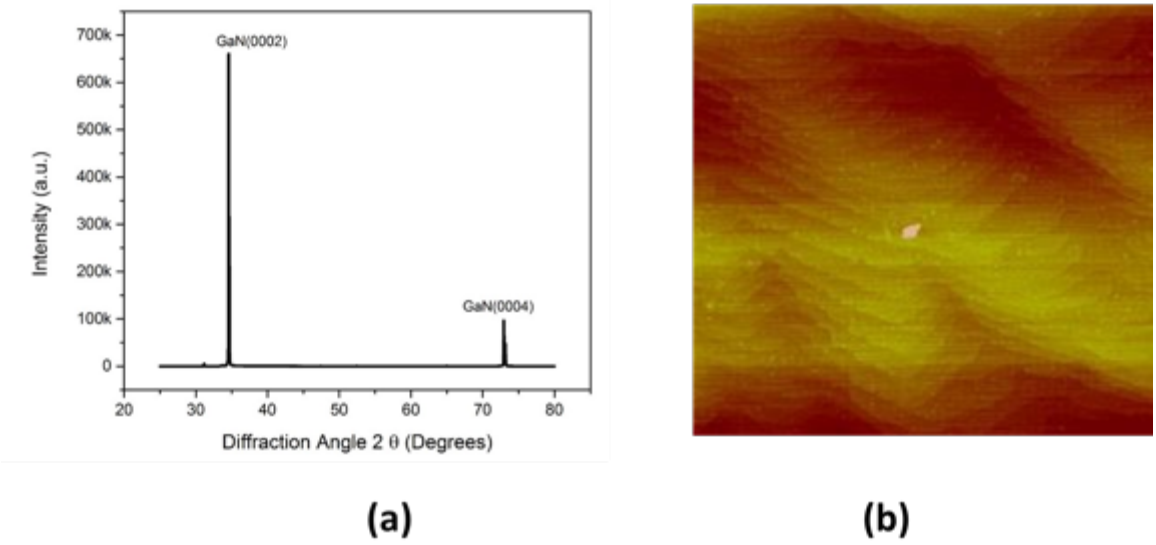


Figure 34(a) X-ray diffraction pattern of the Ammono GaN substrate before AlN growth. (b) Atomic force microscopy image of the (2 μm x 2 μm) GaN/AlN surface showing the atomic steps.

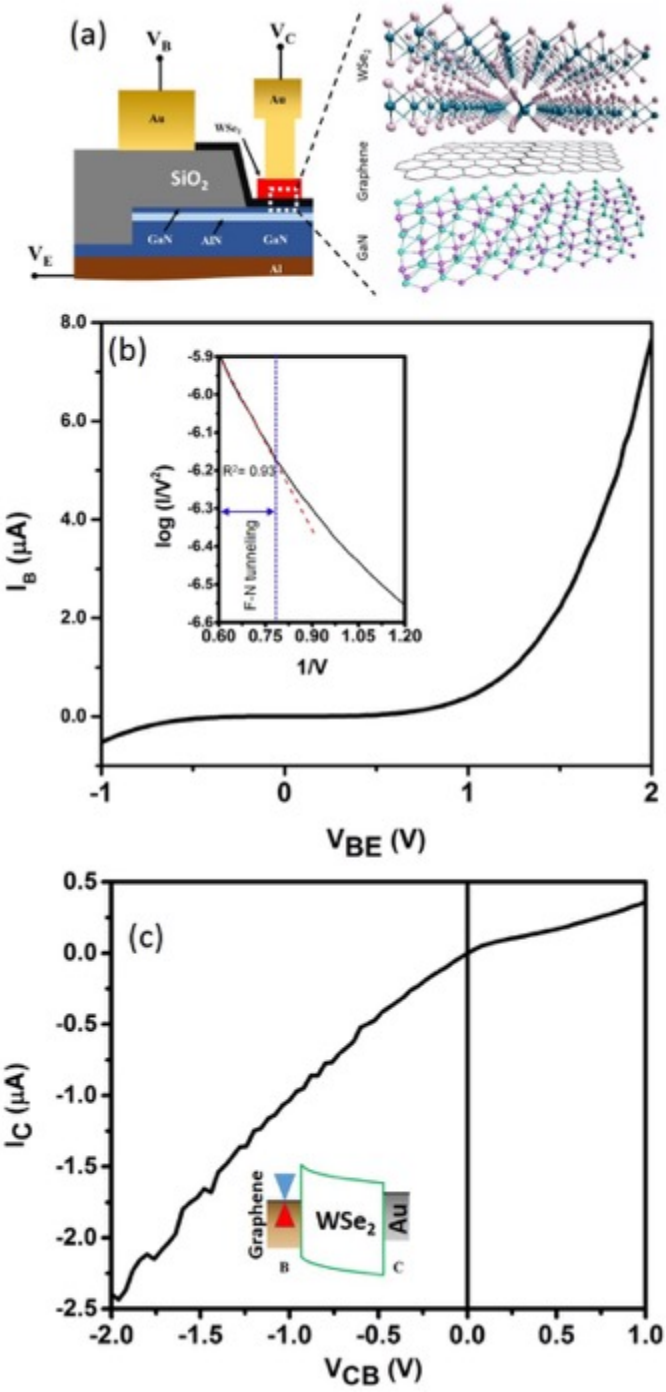


Figure 35: (a) Schematic cross-section of the fabricated GHET with key terminal voltages. *I-V* characteristics of the (b) emitter-base (GaN/AlN/graphene) and (c) base-collector (graphene/WSe_2/Au) heterojunction diode. Fowler-Nordheim fitting (red dashed line) of the diode *I-V* characteristics for the B-E diode is shown in the inset.

The surface of the as-grown heterostructure was pin-hole free and shows atomic steps with a surface roughness of less than 0.5 nm Electron-beam evaporation was used to deposit an Al film on the back-side to contact the 2-DEG at the AlN/GaN interface through heavily doped n-GaN. To prevent the parasitic conduction between the base and emitter, plasma-enhanced chemical vapor deposition (PECVD) deposited thick SiO_2 was used as isolation dielectric (See Figure 35). A monolayer graphene thin film was grown by low-pressure chemical vapour deposition (LPCVD) and then transferred with ethyl-vinyl acetate (EVA) as the supporting polymer.

3.2 Fabrication flow for hot electron transistor

The fabrication process starts with mesa isolation of the AlN structure by BCl_3/Cl_3 plasma based RIE and followed by ebeam evaporation of Ti (10nm)/Al (90 nm) for the emitter contact. The sample is then rapid thermal annealed (RTA) at 550°C for 5 minutes. To prevent parasitic leakage between n-GaN and base contacts, a 200 nm thick Tetraethyl Orthosilicate (TEOS) based PECVD SiO_2 is used as isolation. Via holes are then defined by electron beam lithography followed by a buffered oxide etch to define the active device area. The sample is then treated with HCl solution immediately followed by the transfer of the graphene film.

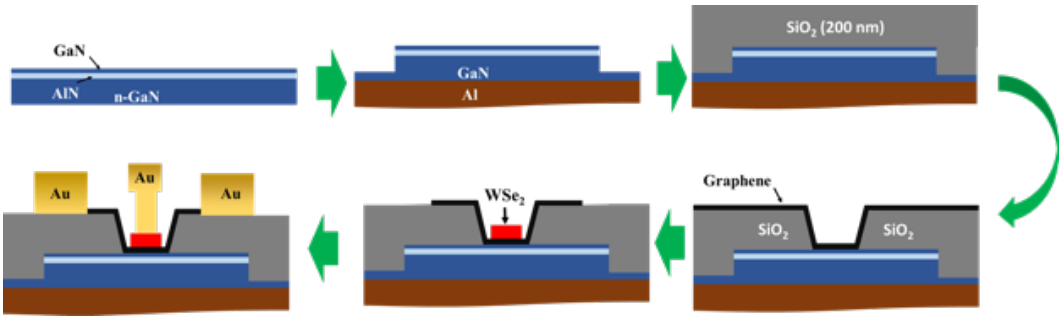


Figure 36 Schematic illustration of HET fabrication process.

A forming gas anneal at 360°C for 3 hours is performed to improve graphene adhesion and for removal of residue from the transfer process. Pre-selected WSe_2 flakes are then transferred on graphene by a dry transfer method. Another forming gas annealing is performed after the transfer to clean the surface and to improve the graphene/WSe_2 interface by removing physio absorbed molecules. Graphene is then patterned by electron beam lithography followed by oxygen plasma based reactive ion etching to define base-collector diode active area. Electron beam cross-linked hydrogen silsesquioxane is used to provide isolation between the base and the collector. Base and collector contacts are then defined by electron beam lithography and ebeam evaporation of 70 nm Au. The final fabricated device is then annealed at 200°C for 3 hours to improve the WSe_2contact. During this anneal a slower ramp rate (10°C/min) is used to avoid contact degradation due to thermal stress. The use of EVA ensured the graphene surface had minimal residue from the transfer process [3].

3.3 Large area CVD Graphene growth and transfer on GaN

High-quality large area monolayer graphene was grown on 25 μm thick Cu foils (99.8%, Alfa Aesar) using an LPCVD method [3]. Before the chemical vapor deposition (CVD) growth, the Cu foils were treated with the commercial Ni etchant to allow reproducible synthesis of clean and continuous monolayer graphene. Under low pressure (1.5 Torr), Cu foil was annealed in a flow of 50 standard cubic centimeters (sccm) of hydrogen (H_2) gas at 1000 °C for 60 min. After the annealing step, 6 sccm of methane (CH_4) gas was introduced to initiate the graphene growth, for 40 min. The graphene growth was carried

out at 1000 °C. To control the graphene growth rate, 20 sccm of H_2 flow was used during the growth period. Once the graphene growth was finished, the CVD chamber was cooled down under 20 sccm of H_2 to prevent oxidation and to minimize hydrogenation reactions of the graphene.

After the growth, an ethyl vinyl acetate (EVA) solution (Sigma Aldrich, vinyl acetate 18 wt%, 10 wt% dissolved in xylene) was spin coated onto the top side of the sample at 4000 rpm for 60 s and dried in an oven at 80 °C for 60 min. The xylene was used to selectively remove the EVA. The EVA was dissolved and washed out by soaking the film in a boiling xylene bath for 15 min and the film was then dried in air. In general, the solubility parameter (δ) could be considered as an important factor in determining the dissolution efficiency of the support/carrier material. In addition, it has been known that an aromatic hydrocarbon, such as xylene, is a more suitable solvent for dissolving/removing EVA. Under our experimental condition, the xylene with a δ, value of 18.2 $MPa^{1/2}$ was chosen to promote a more effective removal of EVA residues from the graphene surface. The xylene is best matched with EVA, and the $|\delta_{EVA} - \delta_{Xylene}|$ value is revealed to be 0.15, indicating that xylene is a "good solvent" for EVA (Figure 37(a)). Thus it is anticipated that the interactions between the EVA polymer and the xylene solvent should be energetically favorable to allow the solvent swell of the EVA polymer chains to completely dissolve away the EVA layer from the graphene surface. Figure 37b-c showed the optical micrograph (OM) and AFM images of transferred graphene on SiO_2/Si substrates using EVA as a supporting material. The OM and AFM images suggest that the EVA-transferred graphene has a much more uniform morphology with less contamination than the graphene transferred by the conventional wet-transfer method.

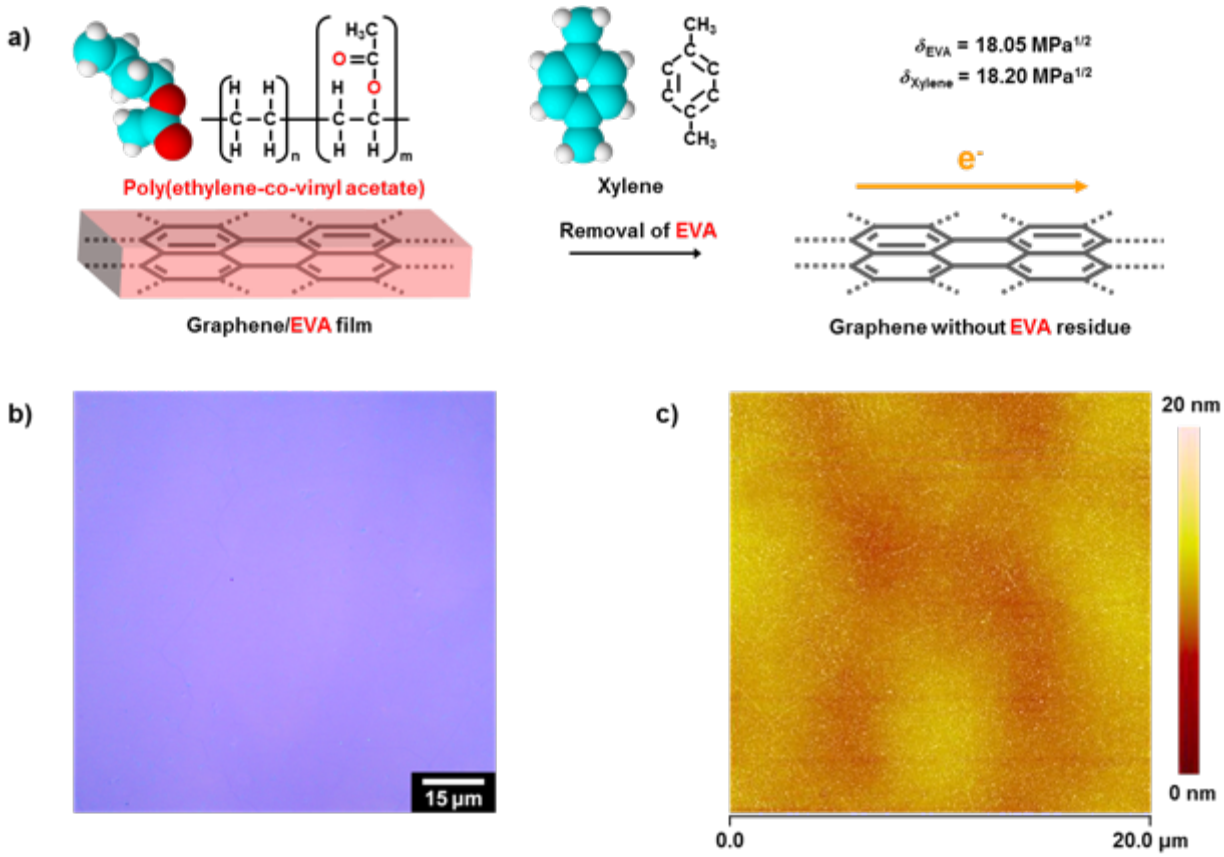


Figure 37. (a) Schematic illustration of the EVA removal mechanism for transferring CVD graphene. (b) The OM image and (c) the AFM image of monolayer graphene transferred to 300 nm SiO2/Si substrate by using the EVA-supported transfer methods.

The transport characteristics of a representative GaN/AlN/graphene diode are shown in Figure 35b. The best performing diode shows a current density of ~ 10 A/cm^2 at V_{BE} = 2 V, which is ~150x higher than the highest reported current value for oxide tunnel barriers at the same bias[68].

3.4 High-$\varkappa$ dielectric as the barrier of HET

Atomic layer deposited (ALD) high-$\varkappa$ dielectrics (i.e. Al_2O_3, HfO_2) has been widely considered as the collector barrier of graphene HETs [57, 58, 118]. One of the advantages of these dielectrics is the potential for large area growth and wafer scale integration of

HETs with existing CMOS technology. However, nucleation of ALD is challenging on graphene surfaces due to the hydrophobic and inert surface of graphene. This problem can be overcome partially by using a thin of air-oxidized metal layers (e.g. Al), functionalized graphene or graphene oxide [70] as the seed layer for relatively thick (> 5 nm) dielectrics which can be used as gate dielectrics. However, the growth of high quality, thin dielectric layers required for HET collector barriers still remains challenging. To compare the performance of the structure of the current work with dielectric barrier devices, we fabricated a test structure with Al_2O_3 as both B-E (~7 nm) and C-B barrier (1nm air-oxidized Al_2O_3 as seed layer plus ~10 nm ALD oxide) as shown in Figure 38. From the diode characteristics shown Figure 38(b) and (c) it is evident that the structure presented in this work with WSe_2 as collector barrier shows superior performance over the device with an oxide barrier with a similar barrier thickness in the same operation bias range. The maximum gain measured in the test device is only ~0.2.

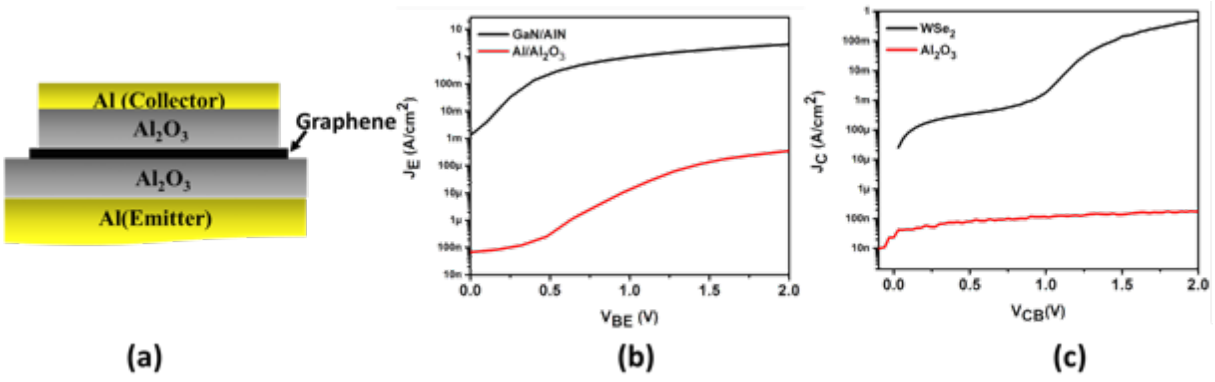


Figure 38. **(a)** Schematic cross-section of the fabricated HET with Al_2O_3 as dielectric barriers (b) J-V comparison of GaN/AlN/graphene and Al/Al_2O_3/graphene diodes. (c) Characteristics comparison showing *Jc* vs V_{CB} between a WSe_2-based and an Al_2O_3-based B-C diode.

3.5 Integration of graphene/WSe_2 heterostructure in HET

The current density can be further increased by using a thinner barrier with improved film quality. The transport through a tunnel barrier can arise from several potential mechanisms, such as direct tunneling of cold electrons through the barrier, Poole-Frenkel emission through the trap states or Fowler-Nordheim tunneling**[68]**. However, both direct tunneling and Poole-Frenkel emission exhibit a very small selectivity for hot electron generation over that for a cold electron, since carrier transport can occur at any energy in the range from the emitter conduction band to the top of the tunnel barrier. However, the Fowler-Nordheim tunneling mechanism, is highly selective for generating hot electrons at the base[68]. According to the Fowler-Nordheim model, the current-voltage has the following relationship:

$$J \propto E^2 exp\left(\frac{-K}{E}\right)$$

where K is a constant dependent on the material parameters, E is the electric field across the barrier and J is the current density. If we plot the diode characteristics as $\log(I/V^2)$ versus $V($ Figure 35b(inset)), a good fit is achieved with the Fowler-Nordheim tunneling model at higher V_{BE}, which confirms that the dominant transport mechanism is Fowler-Nordheim tunneling at that bias range and is favorable for hot electron generation. Obviously, the thickness of the B-C barrier is crucial for enhancing the injection ratio of the hot electron

carriers from the emitter to the collector and minimizing the background B-C cold current emission.

To evaluate the impact of the WSe_2 thickness in our HETs, we fabricated two sets of devices. Device-A: few layer (N=4) WSe_2 barrier and device B: 10 nm-thick WSe_2 (N~16).

Figure 35c plots the transport characteristics of the B-C diode in device A. The heterojunction was formed by pickup and dry transfer of mechanically exfoliated 4-layer WSe_2 flakes on a pre-fabricated B-E stack. The diode characteristics showed a weak rectification with a forward to reverse current ratio of 3 at $|V_{BC}|$= 1 V.

Figure 39 a shows the common-base GHET characteristics under different emitter injection currents. The emitter current values were selected considering the current levels obtained in the B-E diode measurements shown in Figure 35(b). In this configuration, the collector bias was swept while the base was grounded. For negative V_{CB} values in region **I** (forward bias condition of B-C diode), the injected electrons from the emitter encounter the elevated B-C potential barrier as shown in Figure 39b. As a result, the majority of the electrons contribute to the base current after being reflected by the barrier. Maximum reflection occurs at V_{CB}~ -0.75 V, corresponding to the I_C=0 (I_B=I_E) condition. However, if V_{CB} is gradually increased towards the reverse bias condition of B-C diode (**I** → **II**), the potential barrier decreases and gradually becomes energetically favorable for the injected electrons to surmount the barrier. This effect is evident in Figure 39a, where the collector current increases from zero to the emitter current level owing to the decreased width of the base collector barrier. Figure 39c plots α at this bias range, which increases from zero to approximately unity. However, if we further increase V_{CB} (region **III**), the cold electron

leakage increases and becomes the dominating component in I_C,which explains the upturn in current starting at V_{BC} of approximately 0.3 V.

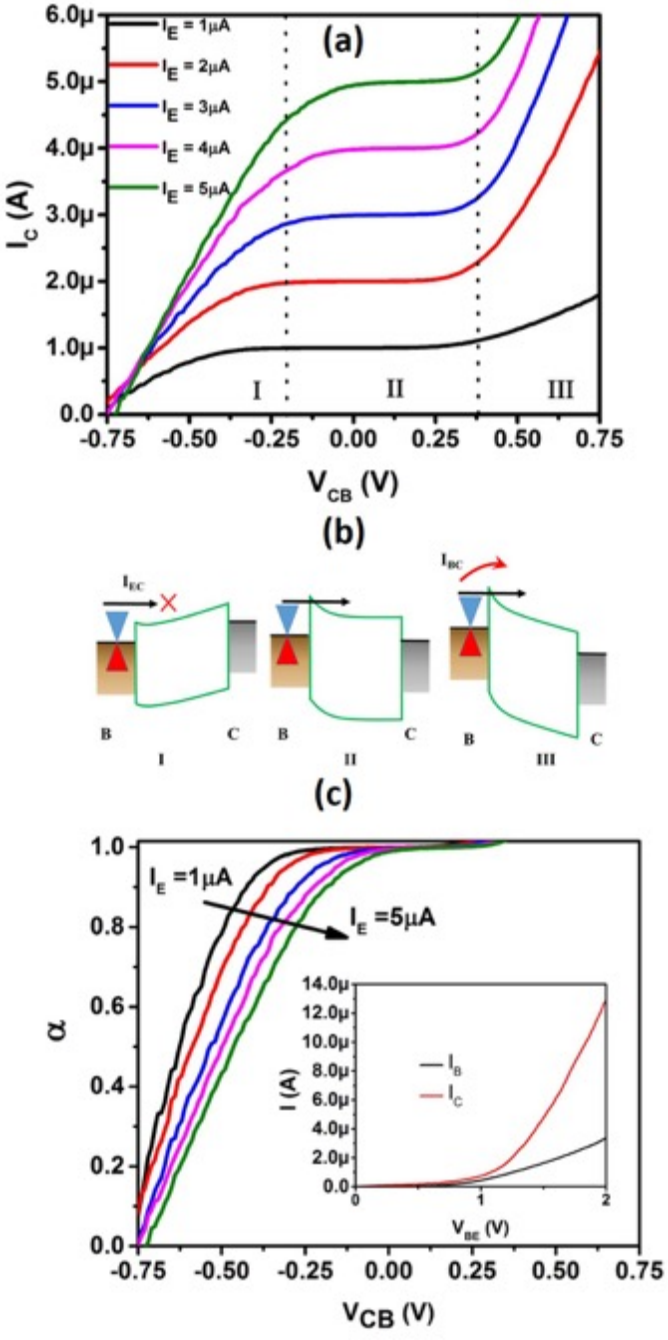


Figure 39(a) Common-base characteristics of the device A and (b) corresponding schematic energy band diagrams in different operating regions(c) Injection ratio for device A for different emitter injection currents. Inset shows the Gummel plot for V_{CB} = 0V.

Although this device shows excellent HET characteristics in terms of α, it has a very limited operating V_{BC} window, which suffers from a poor blocking capability of the B-C junction with an ultrathin WSe_2 barrier. This limitation arises from the fact that the WSe_2 flake used in this device is only 4 atomic layers thick, which allows the hot electron to reach the collector with minimum loss but also, as a blocking barrier, works only for a small bias range (region I and II) with a maximum V_{CB}~0.3 V. Increasing the number of layers can improve the blocking as the larger interlayer resistance between layers of WSe_2[119] would suppress the cold electron transport between base and collector. Therefore, to achieve a better blocking capability, further optimization of the barrier geometry is required.

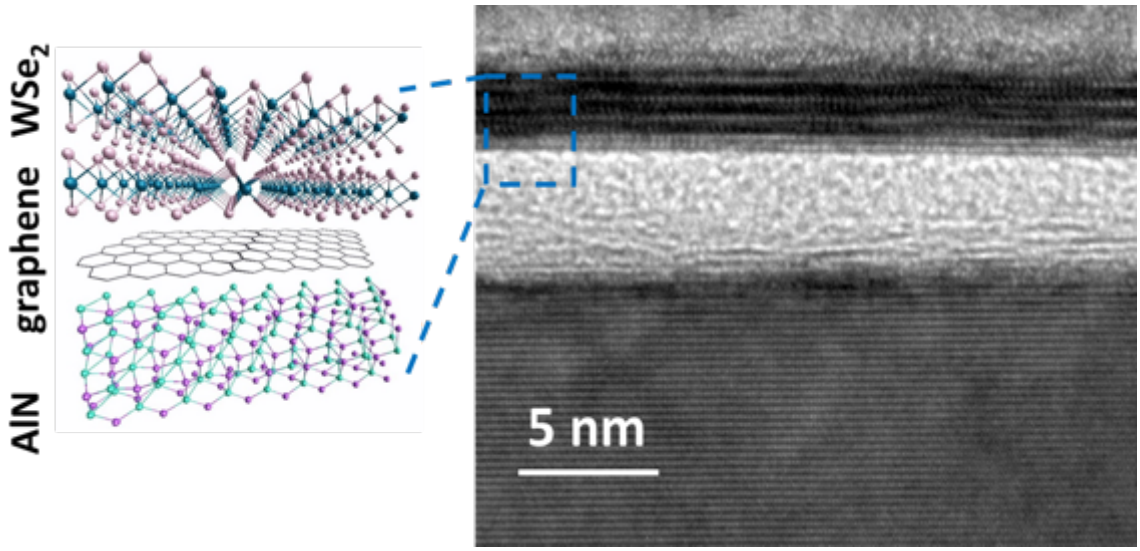


Figure 40 Transmission electron microscope image of a typical HET cross section fabricated in this work. Here, emitter barrier is ~5 nm and collector barrier is 3 monolayer of WSe_2.

To understand the effect of the barrier thickness, we increased the WSe_2 thickness to 10 nm in device B. The B-C diode characteristics showed that the current through the graphene/WSe_2 diode was much smaller (0.5 nA at V_{CB} = 1 V compared with 200 nA in device A) owing to the increased tunneling resistance.

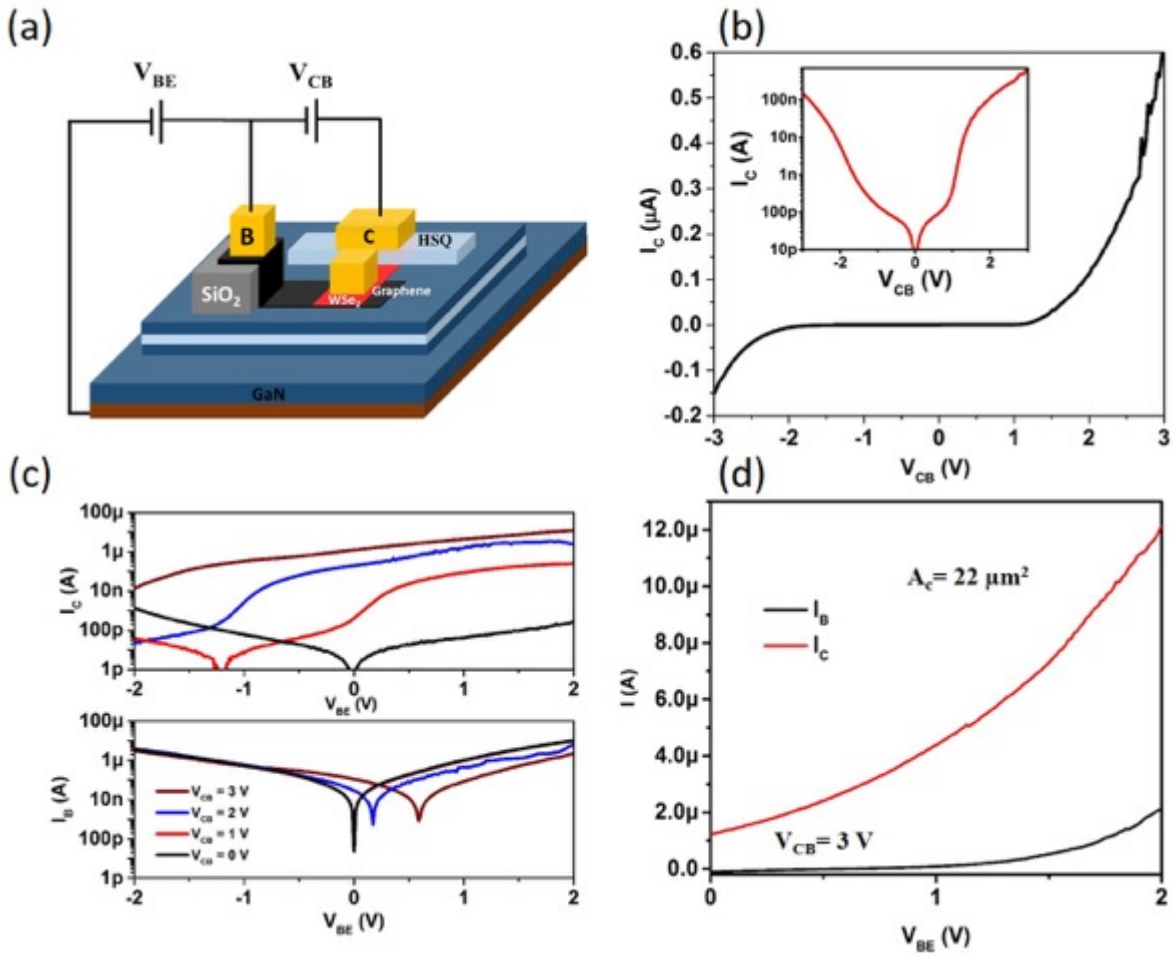


Figure 41(a) Biasing configuration for electrical characterization of a typical HET. (b) *I-V* characteristics of the base-collector diode of device B. Inset shows the same plot on a logarithmic scale (c) I_C, I_B versus V_{BE} characteristics at different V_{CB} values. (d) Gummel plot in the common-emitter configuration for V_{CB} = 3 V.

To characterize the transistor operation, we first biased the device in the common-base mode. Figure 41c plots the base and collector current versus base-emitter voltage at different V_{CB} values. In the absence of an electric field across the B-C junction (V_{CB} = 0 V), the current flow through collector terminal is due to injected carriers from emitter and the current value becomes negligible at V_{BE} =0V. If V_{CB} was increased to higher values, the current magnitude at V_{BE} =2V shows very small change which indicates that collector current is mainly due to hot electron injection from emitter. However, for lower V_{BE} values we notice a significant increase in the collector current indicating the influence of cold electron leakage (I_{BC}) under these biasing conditions.

Next, we biased the device in the common-emitter configuration to study the gain characteristics. Analogous to BJT, the DC current gain (β) in the HET is defined by the following equation in the common-emitter mode:

$$\beta = \frac{I_C}{I_B},$$

For technological applications, it is important to have the current gain at high current values. Figure 41d plots the simultaneous I_C and I_B at V_{CB} = 3 V, where the current value is a maximum and we have gain larger than 1. The resultant current gain at V_{CB}= 3 V was found to be ~5.5 at I_C= 11 μA (J_C= 50 A/cm^2), which is a record among all graphene-base HETs reported in the literature.

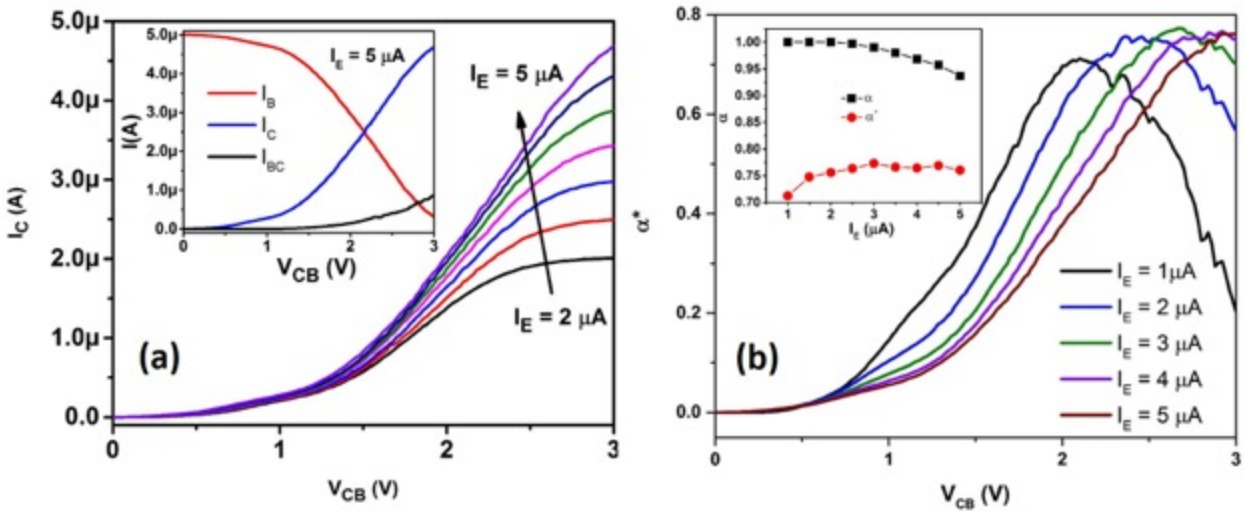


Figure 42 (a) Common-base HET characteristics of the HET at different constant emitter injection currents. The inset compares I_{BC} (the leakage current measured in the two-terminal configuration), I_C and I_B at $I_E = 5\ \mu$A. (b) Modified injection efficiency in the common-base mode for the characteristics in (a). The inset shows a comparison of the injection efficiencies before and after base-collector cold electron leakage correction as a function of I_E.

To understand the origin of the current gain, we characterized the device in the common-base configuration with the emitter terminal used as the constant current source. Since the emitter current value was set to a constant value here, the CB mode measurement could evaluate the hot electron filtering capability of the B-C barrier independent of the B-E heterojunction characteristics. At the low bias regime ($V_{CB} < 0.7$ V), the collector current was negligible, irrespective of the emitter injection current value. This lower collector current value indicated that all the injected electrons from the emitter get reflected at the B-C interface, and eventually thermalize by scattering at the base where they contribute to the base leakage current. At a higher V_{CB}, the energy barrier of the B-C diode becomes

thinner and thus allows the hot electron to pass through the barrier. As a result, the collector current increased monotonically until it reached the emitter current. The inset of Figure 42a compares the base and collector currents at $I_E = 5\ \mu A$ and shows a monotonic increase (decrease) of the collector (base) current, which supports the above explanation of the device behavior. Additionally, we should note that using a thicker WSe_2 layer in device B allows a larger V_{CB} voltage up to 3 V, compared with 0.3 V in device A. However, increasing the thickness of WSe_2 would affect the emission rate of the injected hot electrons as they would have to travel a longer physical path from base to the collector.

The emission rate of the injected hot electrons can be quantitatively evaluated by calculating the common-base injection ratio (α), which represents the ratio of electrons successfully transferred to the collector over the total number of injected electrons from the emitter. Since the emitter current is fixed at a constant value in the CB measurement configuration, the trend of the collector current should represent the value of α which reached to 1 at higher V_{CB}. A unity value of α means all the hot electrons injected from the emitter are being transferred to the collector without being lost in the base owing to scattering or reflection at the C-B barrier (i.e. $I_C = I_{EC}$ and $I_{BC} = 0$). However, at non-zero V_{CB} values, there is a finite current (I_{BC}) flowing between the base and the collector that increases with V_{CB}. The carriers injected from the base to collector are cold electrons, which do not contribute to the amplification. Therefore, calculating α without correcting for B-C leakage overestimates the current gain of the device. Hence, to evaluate the actual amplification potential of the device, we define the ballistic injection efficiency α^* to estimate the ratio of electrons quasi-ballistically transferred from the emitter to collector over the total number of injected carriers. To estimate the ballisticity of the device, we subtracted the B-

C leakage of the device corresponding to $I_E = 0$ A from the collector current obtained at non-zero emitter current levels and we define the ballistic injection ratio as: $\alpha^* = (I_C - I_C(I_E = 0\ A))/I_E$[22]. Figure 42b shows α^* for the same biasing conditions used in Figure 42a. At low V_{CB}, α and α^* are essentially the same since the base-collector leakage is negligible. At high V_{CB} biases, the relative increase of α and α^* is different owing to the increase of cold electron injection from the base. The ballistic injection efficiency of the present device is a competition between the hot electron transfer and the efficiency from the emitter and the cold electron injection from the base. As a result, α^* keeps increasing with V_{CB} until it reaches a peak value where the base collector leakage component starts to dominate the collector current and α^* starts to decrease while α keeps increasing. The maximum value of α^* is independent of the injection emitter current level of the emitter, as shown in the inset of Figure 42b. The maximum value of 0.75 indicates that 75% of the injected electrons from the emitter quasi-ballistically travel to the collector terminal, while 25% of the electrons are lost in the base because of reflection. We noted in device A with ultrathin WSe_2, α was approximately 100% with the price of a very low operation V_{CB}. We can calculate the current gain (β) in device B using the following formula, similar to the heterojunction bipolar transistor, $\beta = \alpha/(1-\alpha)$. The maximum β is found to be ~3, which is consistent with the common-emitter mode β obtained in Figure 41. As the comparison of devices A and B shows, the selection of the collector barrier thickness is a trade-off between the tunneling current density and filtering capability of the barrier. Further in-depth studies based of the targeted device application are required to fully optimize the B-C barrier thickness. Additionally, different layered semiconductors can be studied and benchmarked.

Table 3-1 Benchmarking of different experimental HET performances

	Emitter	**Base**	**Collector barrier**	**J_c(/cm^2)**	**β**	**α**
UCSB'15[36]	GaN/AlN	GaN/InGaN (7nm)	GaN	2.5kA	>1	>0.5
OSU'16[43]	GaN/AlN	GaN (8nm)	AlGaN/GaN	46kA	14.5	0.93
UCLA'15[118]	Si/SiO_2	MoS_2 (0.7nm)	HfO_2	~1 μA	4	0.95
KTH'13[57]	Si/SiO_2	Graphene (0.4nm)	Al_2O_3	~10 μA	0.065	0.065
UCLA'13[58]	Si/SiO_2	Graphene (0.4nm)	Al_2O_3, HfO_2 or Si	~50 μA	~0.78	0.44
KTH'15[68]	Si/TmSiO/TiO_2	Graphene (0.4nm)	Si	4 A	0.4	~0.28
This work	**GaN/AlN**	**Graphene** (0.4nm)	**WSe_2**	**~50A**	**4-6**	**0.75**

We compare the collector current density and DC current gain of different HETs with sub-10 nm base thickness reported in the literature in Table 1. It is evident that the use of a graphene/semiconductor junction improves J_c, α and β when compared with the graphene-base oxide collector HETs. However, the injection efficiency is still 75% owing to leakage of cold electrons from the base to the collector at the operating condition.

3.6 Path towards high performance HET

The HET demonstrated in the previous section demonstrates record performance among the graphene-base HET however the current density is around 3 orders of magnitude lower than state-of-the-art all-GaN HET. It is important to revisit the structure to understand the origin of the low current density.

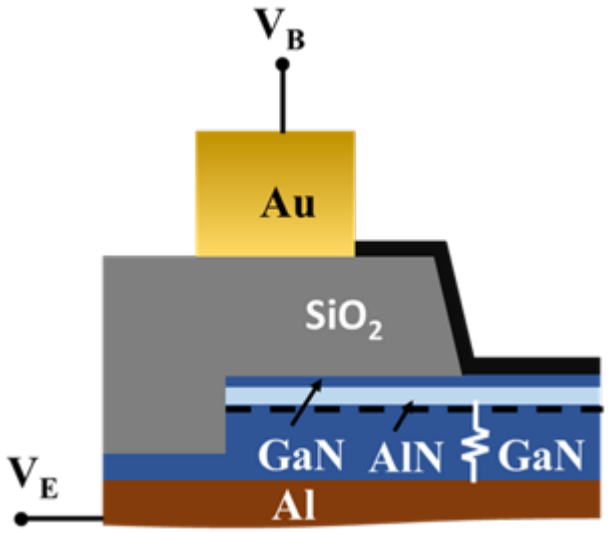


Figure 43 Schematic of the base-emitter diode showing series resistance component due to the presence of thick (~200 nm) UID GaN in the transport path.

For the diode characteristics described in the previous section, the AlN tunnel barrier was grown on Ammono bulk GaN wafer. However, to facilitate high quality growth a layer of 200 nm UID GaN was grown on top of substrate first followed by the growth of tunneling

AlN layer. During the device fabrication emitter contact was formed at the backside of the wafer which adds a significant series resistance in the path of the transport.

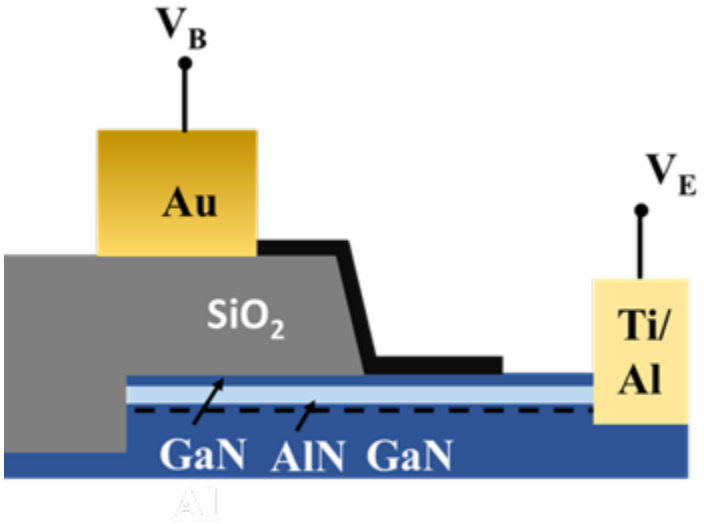


Figure 44 Proposed emitter contact scheme to avoid large series resistance.

Figure 44 shows the proposed emitter contact scheme to avoid a large series resistance along the transport path. In this contact scheme the goal would be to contact the 2-DEG using alloyed tunneling contact trough ultrathin AlN. Moreover, top contact is convenient for probing high frequency devices with coplanar ground-signal-ground (GSG) probes.

The fabrication process starts with the mesa etching of the AlN using BCl_3/Cl_2 ICP chemistry and followed by ohmic metal deposition as shown in Figure 45.

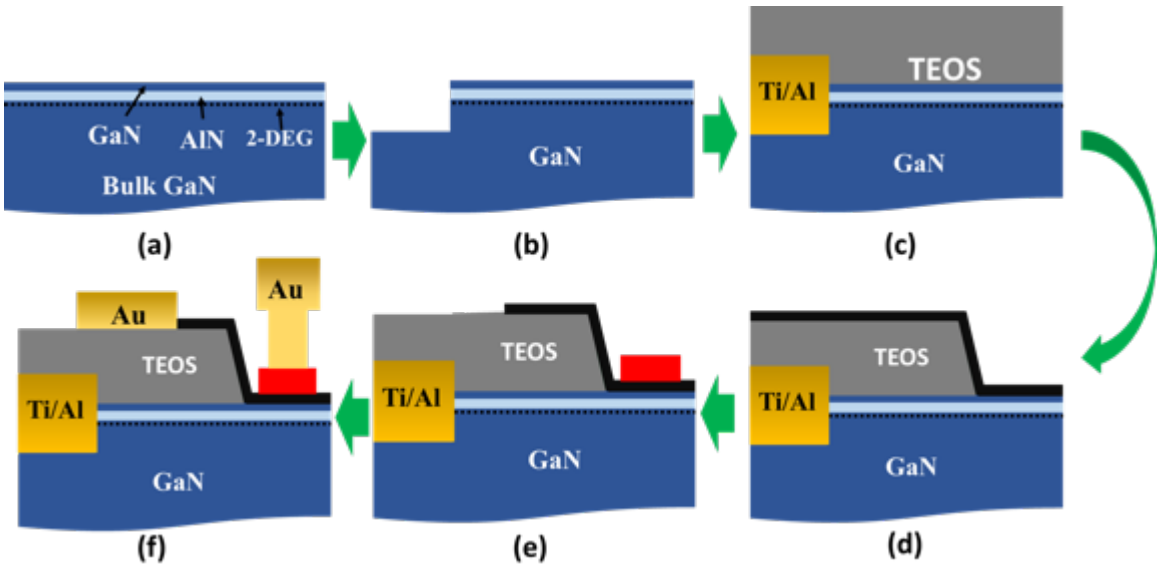


Figure 45 Process flow with the emitter top contact.

After the ohmic anneal the rest of the process is similar to the previous generation. Figure 46 shows a typical B-E diode fabricated using top contact and corresponding Fowler-Nordheim (F-N) fitting of the diode characteristics.

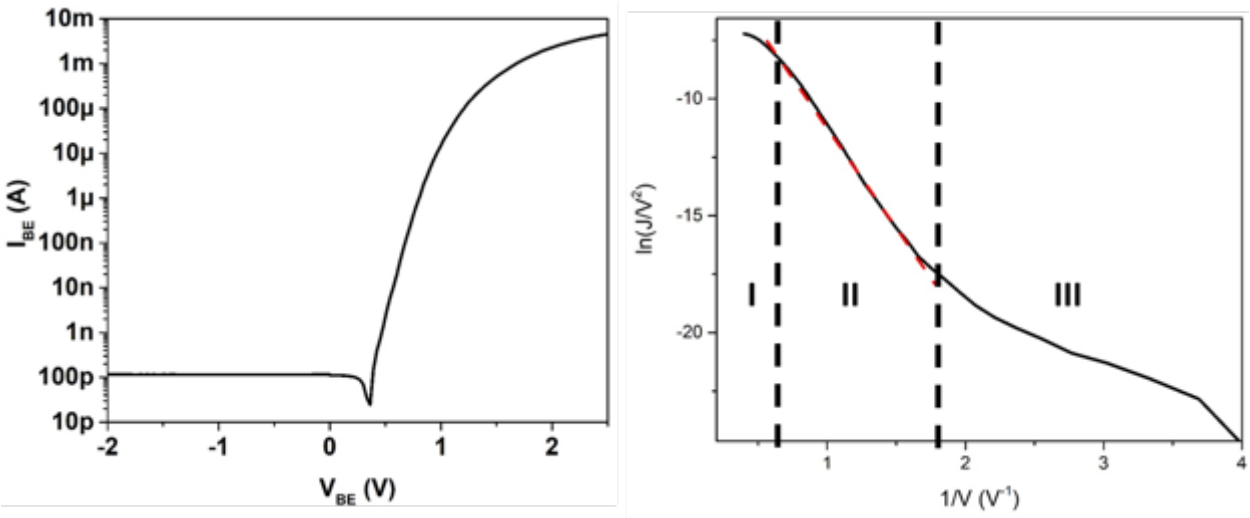


Figure 46 Base-emitter diode characteristics and Fowler-Nordheim tunneling plot.

The B-E diode exhibits excellent rectifying characteristics with a forward to reverse current ratio above 10^7. From the Fowler-Nordheim plot, the diode exhibits three distinct regions. At low bias (region III), the transport is dominated by the leakage current and higher bias (>2 V) the series resistance starts to dominate. In between these regions, the characteristics (region II) show an excellent fit for the F-N equation. To study the effect of barrier thickness scaling, two different set of diodes have been fabricated with different barrier thickness.

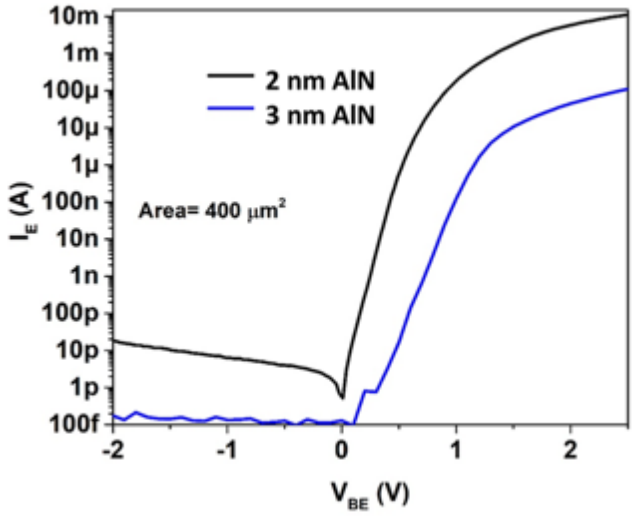


Figure 47 Base-emitter diode characteristics with different tunnel barrier thickness.

The tunnel barrier thickness scaling effectively increases injection current density as shown in Figure 47. The maximum current density achieved for B-E diode with 2 nm AlN barrier is above 2.5 kA/cm^2, more than one order higher than previous generation. Figure 48 shows the temperature dependent forward bias characteristics of the B-E diode. The bias range has been restricted to 2V to avoid the series resistance dominated transport at higher bias.

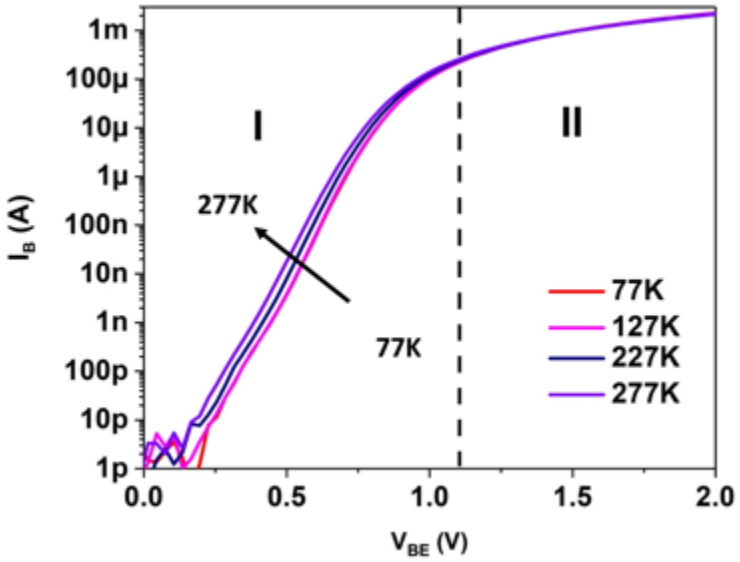


Figure 48 Base-emitter diode characteristics at different temperature.

The measurement has been performed in Lakeshore cryogenic probe station with liquid N_2 as the cryogen. The forward bias characteristics show two distinct regions. In the lower bias range (region I), the diode current shows monotonic increase with the rising temperature from liquid N_2 temperature (77K) to 277K. However, the higher bias shows relatively weaker temperature dependence over the same range. The temperature dependence measurement has also been performed on the graphene/WSe_2 B-C diode as shown in Figure 49. The diode characteristics exhibit four different region when the temperature is varied 77K and 200 K. In both forward and reverse bias, the diode current shows negligible temperature dependence. This could be due to either tunneling or due to the large series resistance. In region II and III, the diode current shows strong

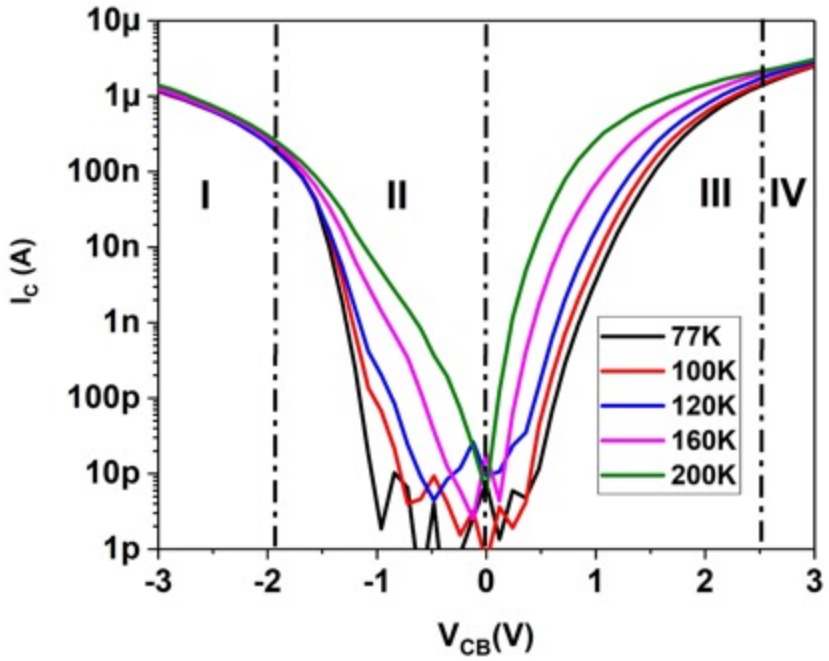


Figure 49 Base-collector diode characteristics at different temperature.

temperature dependence. In region II, the temperature dependence is similar to Shockley-Reed-Hall recombination dominated behavior in tunnel FETs while region III shows similar to band-to-band tunneling region in TFETs. Further in-depth study is required to understand the complete nature of the transport in the base-collector diode.

Figure 50 shows the three terminal common-base characteristics of a typical HET with different constant emitter injection current from 0.2 mA to 1mA at 0.1 mA step. The common-base characteristics shows similar trend to the previous generation device as a function of V_{CB}. However, the injected current density from emitter is order of magnitude higher than the base-collector leakage and hence the collector current is less effected by the cold electron leakage. In this measurement mode, collector current density higher

than 2.5 kA/cm^2 has been achieved, which is 50× higher than the best performing previous generation HET.

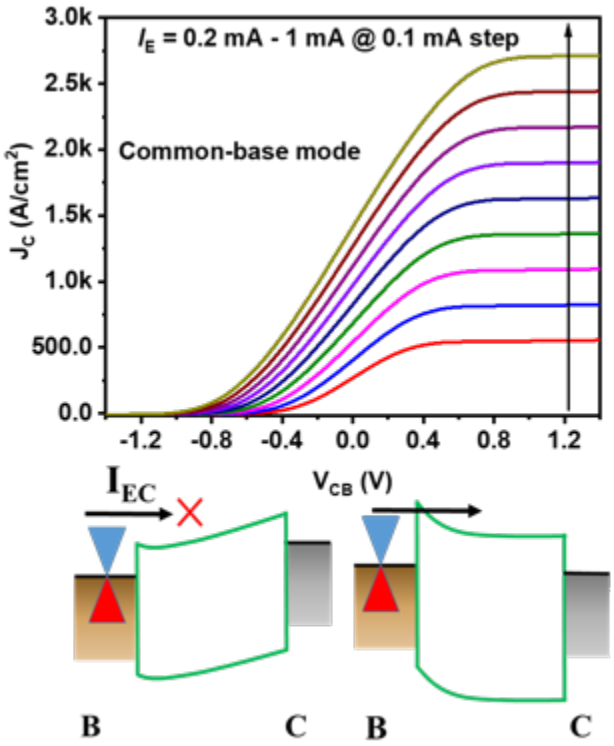


Figure 50 Common-base characteristics of a high performance HET.

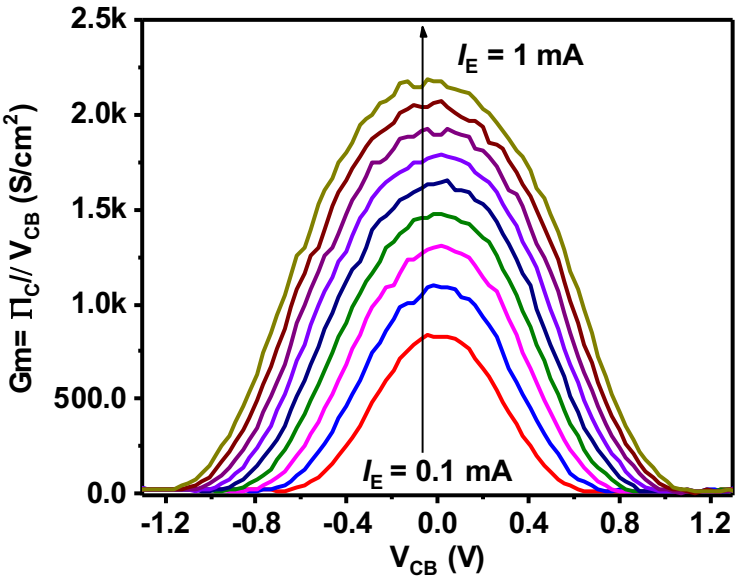


Figure 51 Common-base conductance of the device shown in Figure 50.

In HET, transconductance has been defined as the rate of collector current change as a function of base to collector bias in the common-base mode[120]. Figure 51 shows that the current device can exhibit transconductance higher than 2 kS/cm^2. Finally, the device gain and current density has been benchmarked against the state-of-the-art HETs with base thickness smaller than 10 nm.

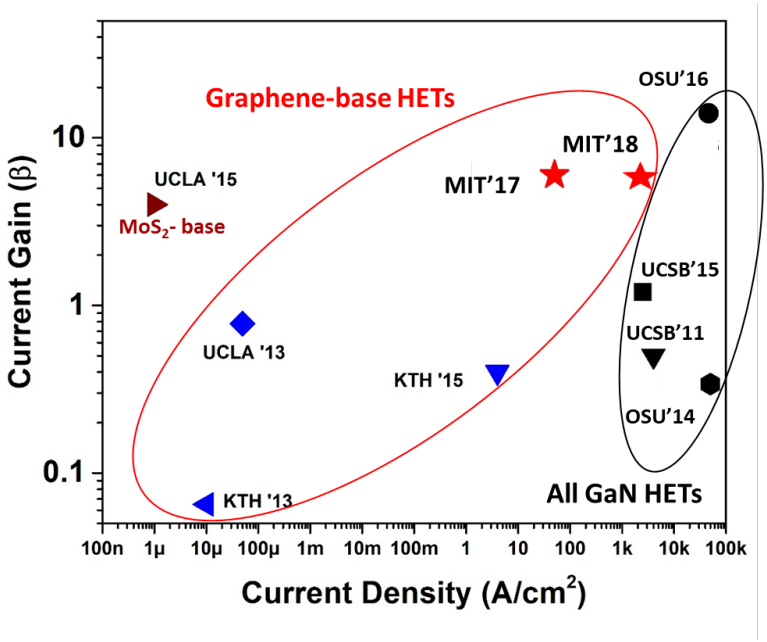


Figure 52 Benchmarking of the current density and gain of the HETs with sub-10 nm base thickness.

The benchmarking plot shows promising progress of the graphene-on-GaN HET with current density within 1 order magnitude of the best performing all-GaN HET.

4 IN-PLANE TRANSPORT IN TRANSITION METAL DICHALCOGENIDES

Semiconductor devices have been the workhorse of innovation and progress in the electronics industry for over 70 years. The research and development in this field has been mainly based on conventional bulk three-dimensional semiconductors like Si, GaAs, GaN, InP etc. However, the successful isolation of single atomic layer graphene by Geim and Novoselov[121] opened up the endless possibility in the two dimensional materials systems which are inherently quantum materials. A plethora of layered two dimensional materials came into the picture following graphene, mostly in the form of transitional metal dichalcogenides (MX_2; where M= Mo, W etc. and X = S, Se, Te). These materials offer unique electrical, optical, chemical and mechanical properties that can enable new applications as well as understanding or realization of novel scientific phenomena. However, it is important to understand the basic transport properties of these materials before exploring any complex device concept or physical phenomena. The simplest device to study the transport properties of two-dimensional materials is the field effect transistors (FETs). However, the majority of studies in the literature is focused on large area electronics and hence the channel length of FETs vary between 50 nm to 10μm. In this chapter, the basic transport properties of two dimensional layer semiconductors will be presented for extremely scaled channel length (15 nm and smaller).

4.1 Short channel effect in MoS_2 FETs

As the transistor channel length has shrunk over the years, short-channel effects have become a major limiting factor to transistor miniaturization. Current state-of-the-art silicon-based transistors at the 14-nm technology node have channel lengths around 20 nm, and several technological reasons are compromising further reductions in channel length. In addition to the inherent difficulties of high-resolution lithography, the direct source-drain tunneling is expected to become a very significant fraction of the off-state current in sub-10-nm Silicon transistors, dominating the standby power. Therefore, new transistor materials and structures that reduce the direct source-drain tunneling are needed to achieve further reductions in the transistor channel length. Transistors based on high mobility III–V materials[122, 123], nanowire field-effect transistors (FETs)[124, 125], internal gain FETs[126, 127] (such as negative capacitance devices) and Tunnel FETs[128] are among those that have been considered to date. More recently, layered 2D semiconducting crystals of transition metal dichalcogenides (TMDs), such as Molybdenum Disulfide (MoS_2) and Tungsten Diselenide (WSe_2), have also been proposed to enable aggressive miniaturization of FETs [129-132]. In addition to the reduced direct source-drain tunneling current possible in these wide-bandgap materials, the atomically thin body of these novel semiconductor materials is expected to improve the transport properties in the channel thanks to the lack of dangling bonds. Some studies have reported, for example, that single layer MoS_2 has a higher mobility than ultra-thin body silicon [133] at similar thicknesses.

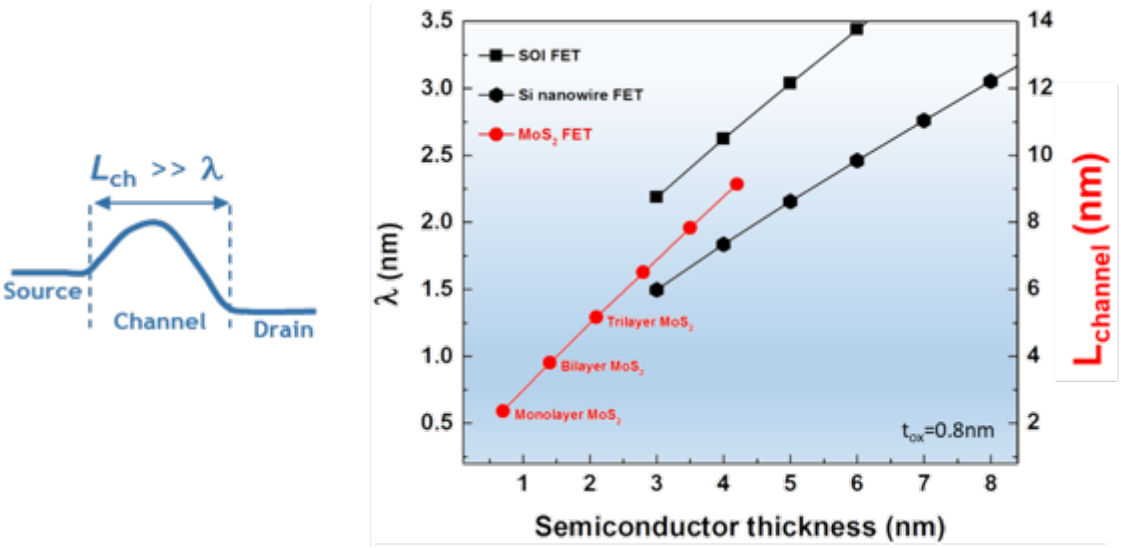


Figure 53: Minimum channel length of MoS_2 FETs before short channel effects become significant.

Moreover, the atomically-thin body thickness of TMDs also improves the gate modulation efficiency. This can be seen in their characteristic scaling length, λ[134]

$$\lambda = \sqrt{\frac{\varepsilon_{Semi}}{\varepsilon_{ox}} t_{ox}.t_{semi}} ,$$

which determines important short channel effects such as the drain-induced barrier lowering (DIBL) and subthreshold swing (SS). In particular, MoS_2, has low dielectric constant ε = 4–7[135, 136] and an atomically thin body (t_{semi} ~0.7 nm × number of layers) which facilitate the decrease of λ while its relatively high bandgap energy (1.85 eV for a monolayer) and high effective mass allow for a high on/off current ratio (I_{on}/I_{off}) via reduction of direct source–drain tunneling[137]. These features make MoS_2 in particular, and wide-bandgap 2D semiconductors in general, highly desirable for low-power sub-threshold electronics. In these applications, the on-current (I_{on}) for a given I_{off} is influenced more by the subthreshold swing (SS) than by the carrier mobility.

One of the major challenges for short channel MoS_2 FETs (in general 2D materials FETs) is the appropriate access region thickness. Due to lack of substitutional doping technique in 2D materials, the source and drain access regions are essentially bulk three dimensional metals[138] deposited by electron beam or other evaporation techniques. The work function of these metals is chosen in such way that the Schottky barrier height is small enough to provide "ohmic" like behavior. This technique works well for long channel transistors where the distance between electrodes is far enough to avoid any negative effect.

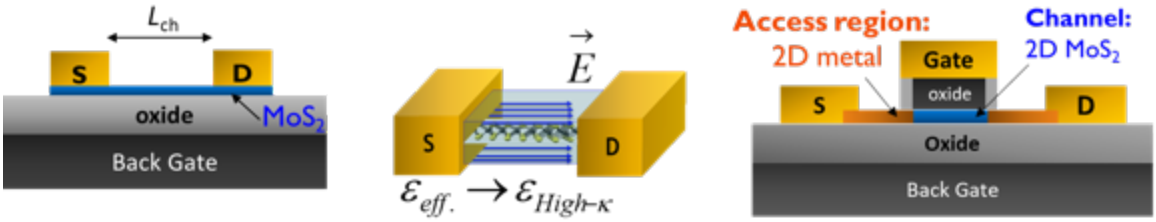


Figure 54: (a) Schematic diagram of a typical 2D materials FET. (b) Electric field profile if the thickness of access region is much higher than the channel (c) Proposed device schematic.

In case of the extremely scaled L_{ch} devices, the electric field lines will be mostly confined inside the high-$\varkappa$ dielectric environment and the effective dielectric constant of the transistor would be dominated by the dielectric constant (i.e. $\varkappa$ = 20-25 for HfO_2) of the gate dielectric. In this structure, there would be a little benefit in terms of SCE due to the low-$\varkappa$ of MoS2. To take full advantage of this, the access region should be as thin as the channel for short channel two-dimensional transistors. This can be achieved by using two dimensional metals (i.e. graphene, metallic phase MX_2etc.) as the access region for two-dimensional semiconductor channel FETs. In the following sections, two different approaches for 2D access region will be discussed.

4.2 Graphene contacted 15 nm channel MoS_2 FET

Monolayer graphene is an excellent candidate for 2D metallic access region due to its extraordinary conductivity, which can be tuned by controlling the doping. Micromechanically exfoliated or CVD graphene back contacts have been used to contact MoS_2 FETs previously [139]. However, this approach requires the graphene pre-patterning before transferring MoS_2 on it. The polymer residue from graphene patterning may degrade the quality of the contact. Here, we demonstrate the selective patterning of monolayer graphene on monolayer MoS_2 without damaging it.

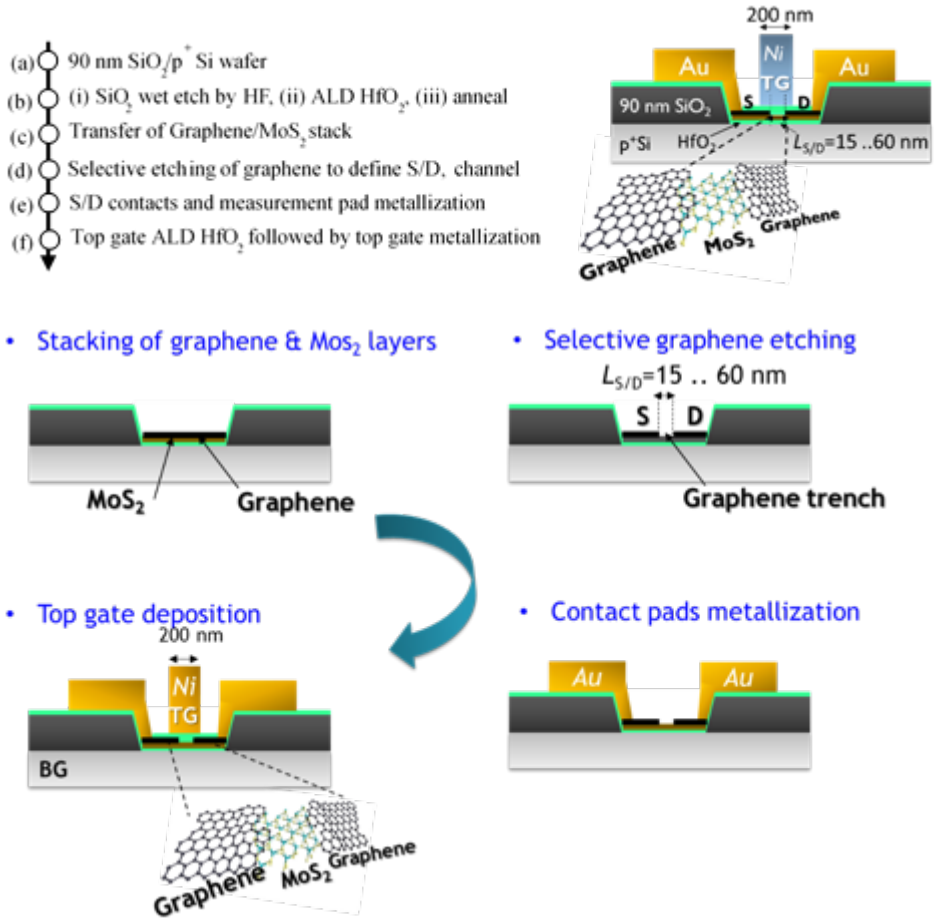


Figure 55 (a) Process flow for graphene-contacted MoS_2 FETs (b) Final device schematics (c) Schematic of key process steps.

4.2.1 MoS_2 FET Fabrication Technology

The key steps for fabricating MoS_2 FETs with graphene S/D contacts, as well as a schematic of the devices, are shown in Figure 55. Typically, heavily doped Si substrates coated with ~300 nm of SiO_2 are used as the back-gate stack in 2D FETs. The reasons for using such a thick oxide layer are twofold: to obtain sufficient optical contrast to locate micrometre-wide flakes, and to avoid large gate leakage, because the Si substrate is a global back gate with 100% overlap with the source/drain contacts and measurement pads.

To enhance the performance of the transistors and improve gate efficiency, we need to increase the gate dielectric capacitance while keeping the gate leakage current as low as possible. Herein, a simple solution is used to solve this problem: we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using the thick SiO_2 layer. In this configuration, the transistor benefits from a global back gate that provides low contact resistance, and the gate leakage current is also reasonably low.

For the scaled gate dielectric devices, 30 × 30 μm via holes were defined on a 90-nm SiO_2/Si substrate by electron-beam lithography. These via holes were then wet etched followed by atomic layer deposition of 10 nm of HfO_2 using tetrakis (dimethylamido)-hafnium (IV) and water at 250 °C. The sample was annealed in forming gas at 400 °C to reduce the bulk oxide traps. After preparing the back-gate dielectric stack either a CVD-grown monolayer or a mechanically exfoliated 4-layer MoS_2 was transferred into the active area. Subsequently, a monolayer graphene was transferred onto the MoS_2 layer. The fabrication of the device continued with patterning and selective etching of the

graphene. High resolution electron beam lithography (Elionix ELS-125) has been used patterning with Poly (methyl methacrylate) (PMMA) as the resist. Typically, room temperature mixture of Methyl isobutyl ketone and Isopropanol (1:3 or 1:2) is used for PMMA development. However, the back scattered electrons may cause broadening of the pattern during the electron beam exposure step, which could be significant in the process. To avoid this issue a common methodology is to lower the development temperature [140]. The thickness of the PMMA also plays a critical role to achieve ultra-scaled patterns. Table I shows the different parameters used in this experiment.

Table 4-1The conditions for electron beam lithography in Elionix ELS-125

PMMA thickness	25 nm
Field size	250 μm
No of dots	500000
Resolution	0.5 nm
Development temperature	-15˚C

Using this optimized process, high resolution PMMA trenches ranging from 60 to 15 nm have been achieved. The sample is exposed to indirect oxygen plasma as opposed to the standard direct plasma typically used for etching graphene. By controlling the duration of plasma exposure, a controlled and selective process has been achieved which can successfully etch the monolayer graphene while protecting the MoS_2 underneath. Details on the pulsed plasma etch process are reported in [141].

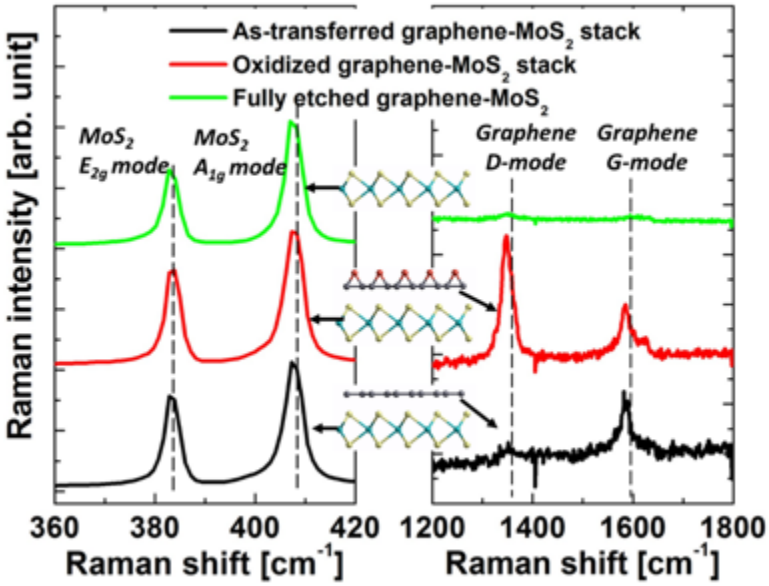


Figure 56: Raman spectra of graphene/MoS_2 heterostructure during etching steps.

Figure 56 shows the Raman spectra of a control graphene/MoS_2 stack without PMMA patterning during the plasma etching process. In the bottom spectrum, characteristic peaks for MoS_2 (E_{2g} and A_{1g}) and graphene (G) peaks are visible while the D peak of graphene is negligible. The magnitude of the D peak corresponds to the presence of defects in the graphene layer. The spectrum in middle has been collected after graphene has been fully oxidized after few O_2 pulses. The presence of strong D peaks denotes oxidation and presence of defects. After an additional O_2 pulse, graphene is now fully etched (no graphene Raman peaks are present) while MoS_2 peaks are minimally affected by this plasma process as evident in the Raman spectrum. This experiment confirms the selectivity of the controlled etching process. This etching process has been applied to the patterned samples to define the channel for MoS_2 FET.

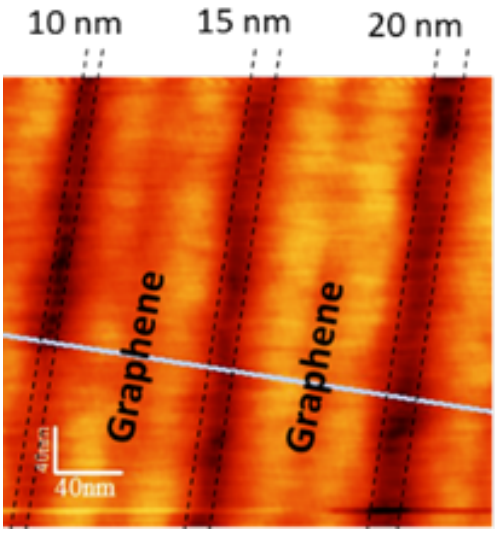


Figure 57: Atomic Force Micrograph of the 10, 15 and 20 nm graphene slits developed using the optimized method after PMMA removal in forming gas annealing.

After dry removal of the PMMA with a forming gas anneal, 1 nm air-oxidized Al_2O_3 was deposited as the ALD seed layer followed by 10 nm ALD HfO_2 and 50 nm of Ni onto the channel to build the top gate (TG).

4.2.2 Long channel MoS_2 FET characteristics

To understand the short channel effects of the MoS_2FETs, it is important to establish a baseline long channel FET process with a scaled gate dielectric, which can be used to benchmark the device performance as the device dimensions are scaled down. The fabrication flow of the long channel devices (Figure 58) is similar to the one in short channel devices except for the access contact metal where Au would be used as the access metal instead of graphene.

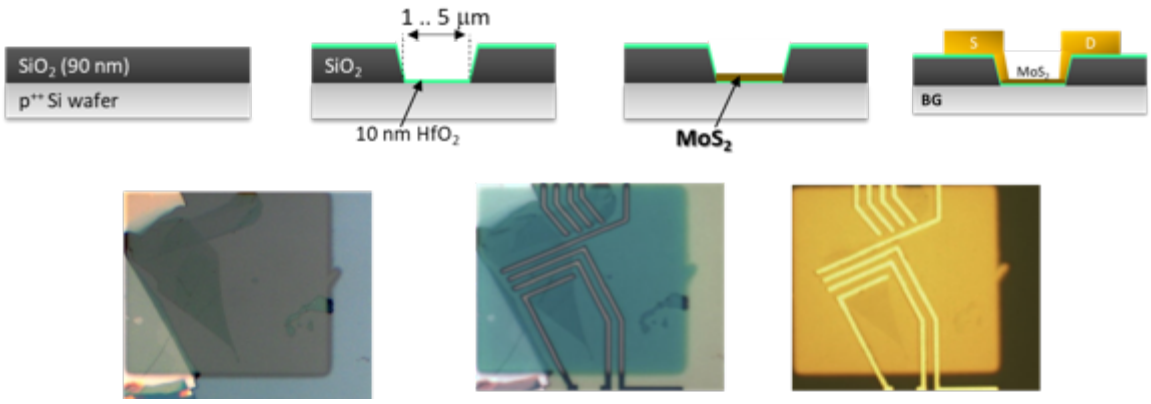


Figure 58 : (Top) Schematic process flow for long channel MoS_2 FET fabrication. (Bottom) Optical image of the long channel MoS_2FET fabrication process.

MoS_2 is transferred by wet and dry transfer method for CVD and exfoliated materials, respectively. The interface quality between the semiconductor channel and the oxide plays a crucial role in all kind of FET devices. The presence of interface trap and defects can degrade the transistor performance. Capacitance-voltage (C-V) characteristics is a simple but powerful method that can reveal many important information about the device. An MIS capacitor was fabricated with MoS_2as the semiconductor and with the 10 nm HfO_2 described before as the insulator. It is evident form the C-V characteristics of the as-fabricated device (Figure 59 (a)) that the interface between MoS_2 and HfO_2 is not ideal and the transition from depletion to accumulation is not steep which is the signature of high quality trap-free interface. The interface can be significantly improved by a post metallization annealing at 360°C as shown in the C-V characteristics in Figure 59(b). A sharp transition from depletion to accumulation can be observed at low

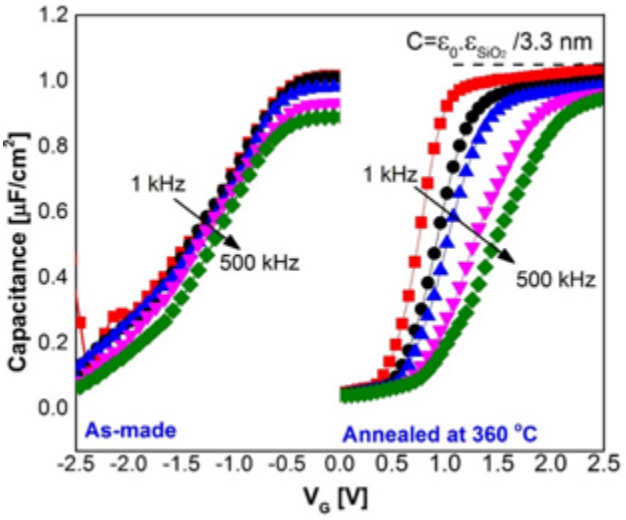


Figure 59 : Capacitance-voltage characteristics of the (a) as-fabricated and (b) annealed MoS_2 MIS capacitor as at different frequencies.

frequency which indicates improvement of the interface quality. The capacitance value in the accumulation region can be used to extract the equivalent oxide thickness (EOT) of 3.3 nm for the gate stack (10 nm HfO_2+ native SiO_2).

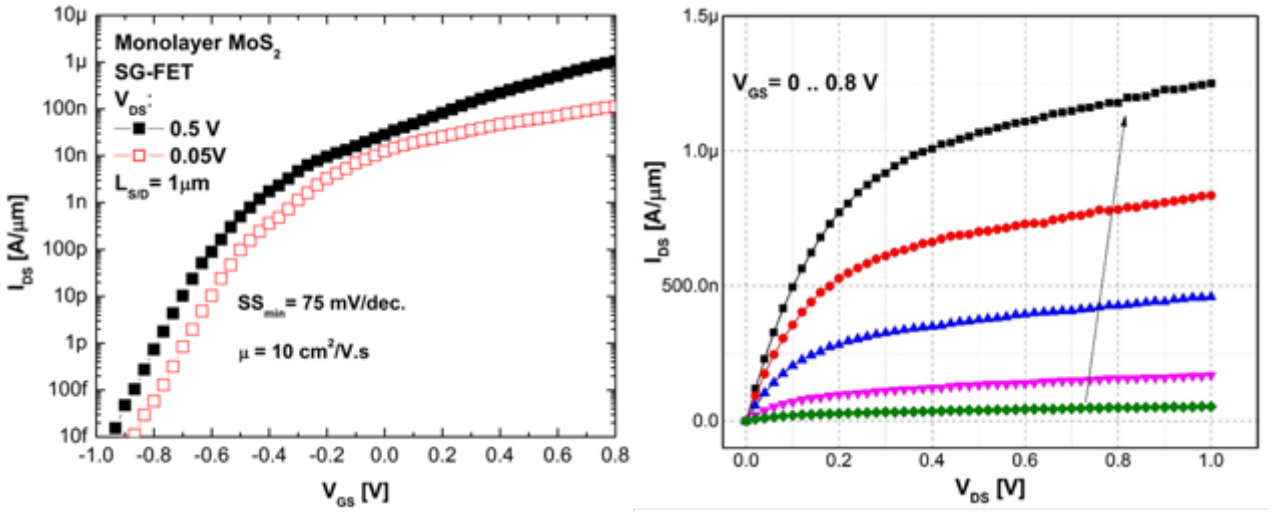


Figure 60 : (a) Transfer and (b) output characteristics of the long channel (L_{SD}= 1 μm) MoS_2 FET.

Figure 60 shows the transfer and output characteristics of the single-gate (SG) long channel MoS_2 FET. The monolayer FET had a room-temperature I_{on}/I_{off} in excess of 10^7 due

to the relatively wider energy bandgap (E_g ~ 1.8 eV) and $SS_{min.}$ =75 mV/dec. The field-effect mobility (μ_{FE}) of the FET can be extracted to be 10 $cm^2/V.s$ .The combination of transfer characteristics and C-V confirm that the n-type MoS_2-FETs operate in the accumulation-mode. The output characteristics shows current saturation at higher V_{DS} as expected from a long FET.

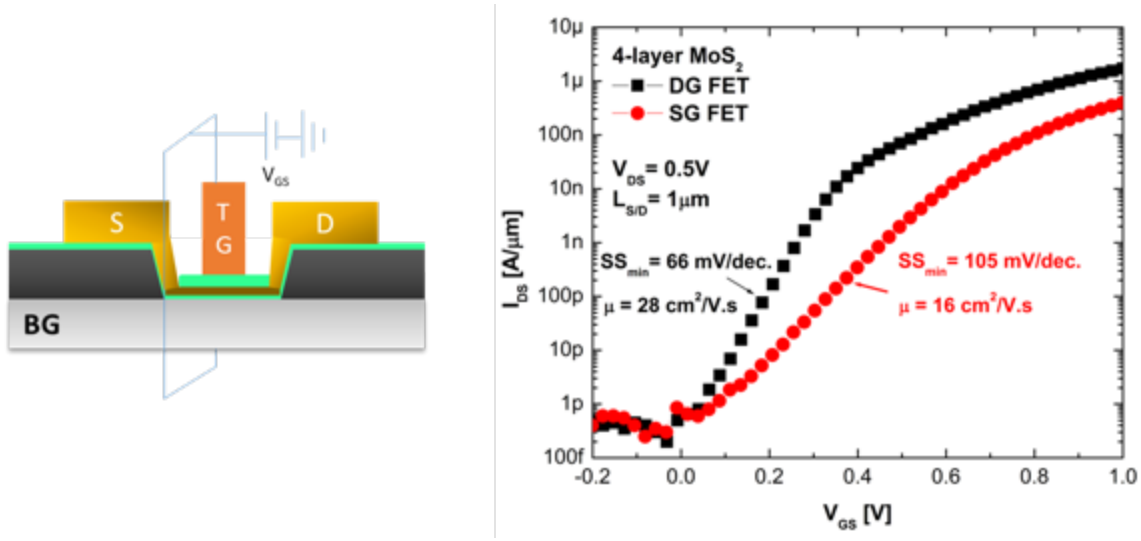


Figure 61 : (a) Schematic of a double gate MoS_2 FET and (b) transfer characteristics of 4-layer SG and DG FET.

For electrical performance, few layer (3-4) MoS_2 is considered to be better than monolayer due relatively lower bandgap, density of states and higher resistance to environmental effect during fabrication. To improve the device performance an FET with 4-layer (~ 2 nm) channel has been fabricated. Figure 61 shows the transfer characteristics of long channel ($L_{S/D}$=1 μm) 4-layer MoS_2 FETs. The SG 4-layer FET had a smaller I_{on}/I_{off} and a larger SS_{min} (105 mV/dec) compared to the monolayer FET. However, the field effect mobility is higher (10 $cm^2/V.s$) than the monolayer case. In layered materials, the inter-layer resistance between layers is significantly high which can screen the electric field and hence, weaken the control of channel electrostatics by the gate. This issue can

be significantly improved by adding a top gate which provides additional control of the channel electrostatics. The 4-layer DG FET shows significantly improved performance in terms of near-ideal SS_{min} 66 mV/dec, I_{on}/I_{off} to ~10^7 and μ_{FE} ~ 28 $cm^2/V.s$. These long channel devices confirm the robustness of the fabrication technology which is very important for short channel device study.

4.2.3 Short channel MoS_2 FET characteristics

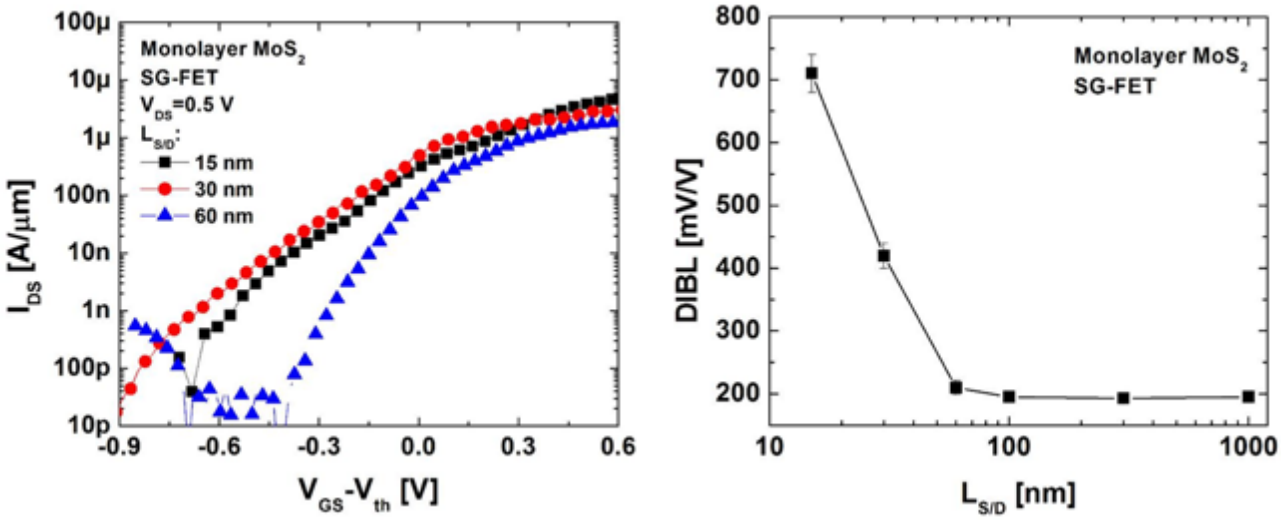


Figure 62 : (a) Transfer characteristics of 15 nm, 30 nm and 60 nm monolayer MoS_2 SG FET (b) DIBL as a function of channel length.

While there have been a number of theoretical works in the scalability or the short channel effects in MoS_2 FETs, the shortest channel length demonstrated prior to the current work was 32 nm. Short channel MoS_2 FETs have been fabricated using the process described in previous section with minimum channel length of 15 nm. The transfer characteristics of 15, 30 and 60 nm SG monolayer MoS_2 FETs with graphene contact are compared in Figure 62. The devices show relatively lower I_{on}/I_{off} ~ 10^5.

However, Drain Induced Barrier Lowering (DIBL) and SS degradation can be used to quantify the short channel effect.

MoS_2 shows good robustness against SCE down to L_{SD} of 60 nm. When L_{SD} is scaled below 60 nm the SCE becomes significant as the I_{off} increases due to enhanced source to drain tunneling in the off state. This effect is being manifested by the SS degradation and DIBL upturn. The SS degrades from 75 mV/decade in 60 nm L_{SD} to 180 mV/decade and 200 mV/decade in 30 nm and 15 nm L_{SD} respectively.

However, as expected, the SCE was stronger in the SG 4-layer FET where the electrostatic control of the gate is relatively weaker, resulting in larger SS and I_{off}. Nevertheless, the subthreshold characteristics of 4-layer MoS_2 could be significantly enhanced by integrating a TG, taking into account that 4-layer MoS_2 has better potential for digital application due to its higher mobility resulting from its higher density of states and lower interface effects compared to monolayer MoS_2 [6]. In addition, the threshold voltage, V_{th} of 2D materials FETs can be affected by the surface doping of physio absorbed molecules and fabrication related surface modification.

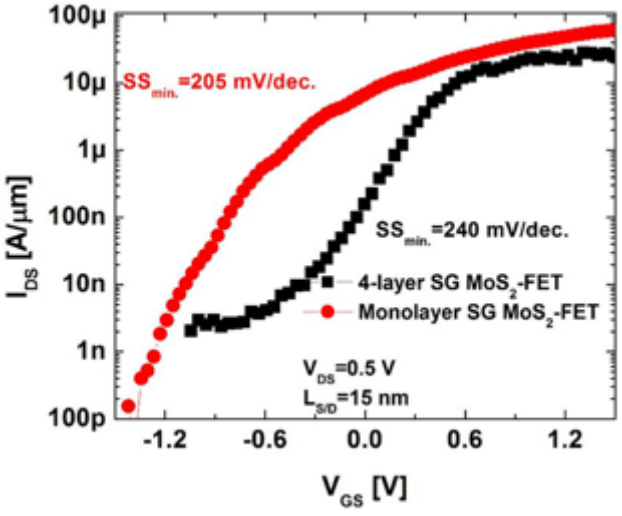


Figure 63: Transfer characteristics of monolayer vs 4-layer MoS_2 FET for L_{SD} = 15 nm.

In this regard, 4-layer FET shows better immunity to the surrounding effects as manifested in the V_{th}.

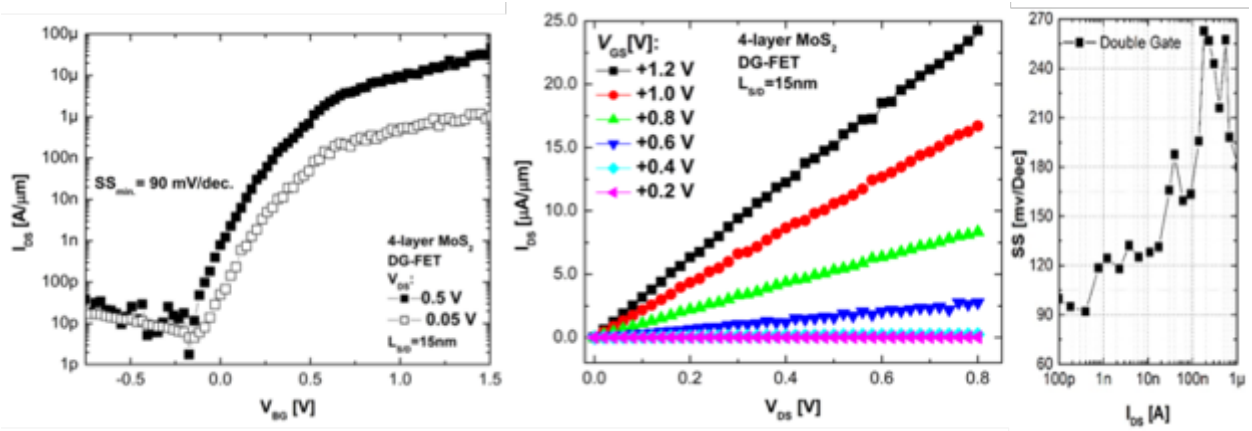


Figure 64: (a)Transfer, (b) output and (c) subthreshold characteristics of double gate 4-layer MoS_2 channel FET with L_{SD} = 15 nm.

Figure 4-12 shows the device characteristics of a 4-layer MoS_2-FET in the DG configuration. The MoS_2 FET had excellent I_{on}/I_{off}=~10^6, I_{on}=~50 μA/μm and $SS_{min.}$ =90 mV/dec. at V_{DS}=0.5 V. The improved SCE are expected from the characteristics length of the device. For this device, the L_{min}(=4λ) needed to incur significant SCE in single gate configuration was ~17 nm (>$L_{S/D}$=15 nm), while for double gate configuration $L_{min.}$ =~11 nm, which is in agreement with the downshift of the upturn point in DIBL to $L_{S/D}$=15 nm with a relatively low maximum. The DIBL values indicate that the SCE was suppressed.

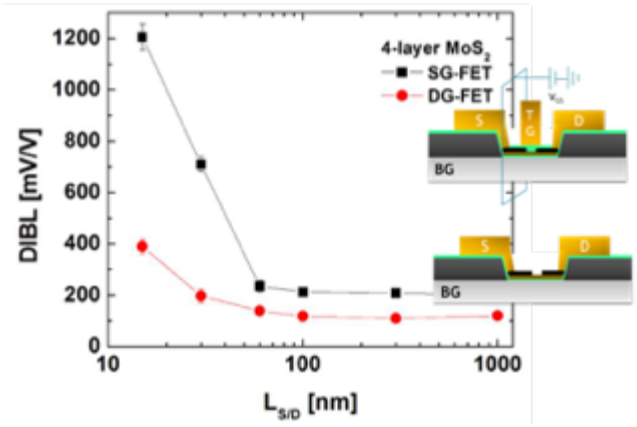


Figure 65: DIBL as a function of L_{SD} for 4 layer MoS_2 in single and double gate configuration.

The need for a thin access region can be understood from a study of the DIBL characteristics. Figure 65 shows the DIBL comparison between graphene vs conventional metallic access region as a function L_{SD} for single gate MoS_2 FET. It is evident that the use of atomically thin graphene contact suppresses the SCE significantly in MoS_2 FETs.

4.3 Sub-10 nm channel MoS_2 FET with phase-engineered contact

The high contact resistance of 2D FETs has been a major bottleneck for realization of high performance devices. This high resistance is due to the lack of substitutional doping technology for the contact regions. However, these materials can be stabilized in different crystallographic phases which leads to different materials properties and new opportunities for engineering the access regions of devices.

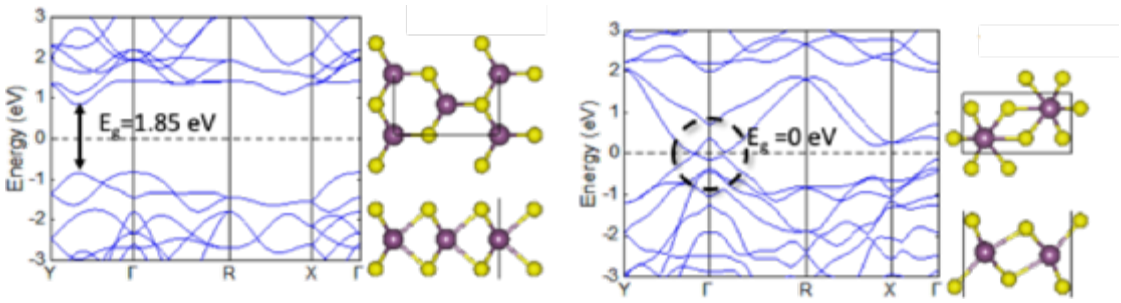


Figure 66: Band and crystal structure of monolayer (a) 2H-MoS_2 and (b) 1T- MoS_2 obtained from density functional theory (DFT) calculations.

Conventional semiconducting MoS_2 has a hexagonal 2H structure with a bandgap of 1.85 eV, although it can also exist in octagonal 1T and 3R phase. The 1T phase of MoS_2 is particularly interesting because it behaves like a metal due to the gapless nature of its band structure.

To minimize the contact resistance, a seamless junction between the metallic phase of MoS_2 (1T) and its semiconducting phase (2H) [142-144] can be used since these two phases have very small (0.5%) lattice mismatch.

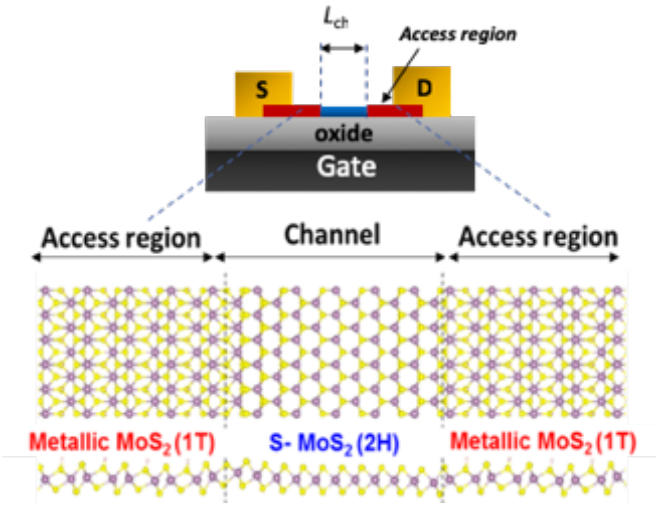


Figure 67: Schematic diagram of the proposed MoS_2 FET with seamless 2H/1T junction.

Ideally, the proposed seamless junction device can be fabricated by selective growth of different phases of MoS_2 in the contact and the channel region. However, the growth technique of MoS_2 is still not mature enough to realize this technology at the sub-10 nm length scale. Alternatively, the transition from the 2H- to the 1T-phase can be triggered by chemical treatment by organolithium compounds. Kappera *et al*. has shown that exposing 2H MoS_2 to *n*-butyllithium (*n*BuLi) solution[145] can induce the phase transformation to 1T phase in μm length scale. The pure 1T-phase is unstable, and undergoes a structural transition to the dynamically stable 1T'-phase[145] which has distorted octahedral crystal structure.

4.3.1 Chemical phase transformation of MoS_2

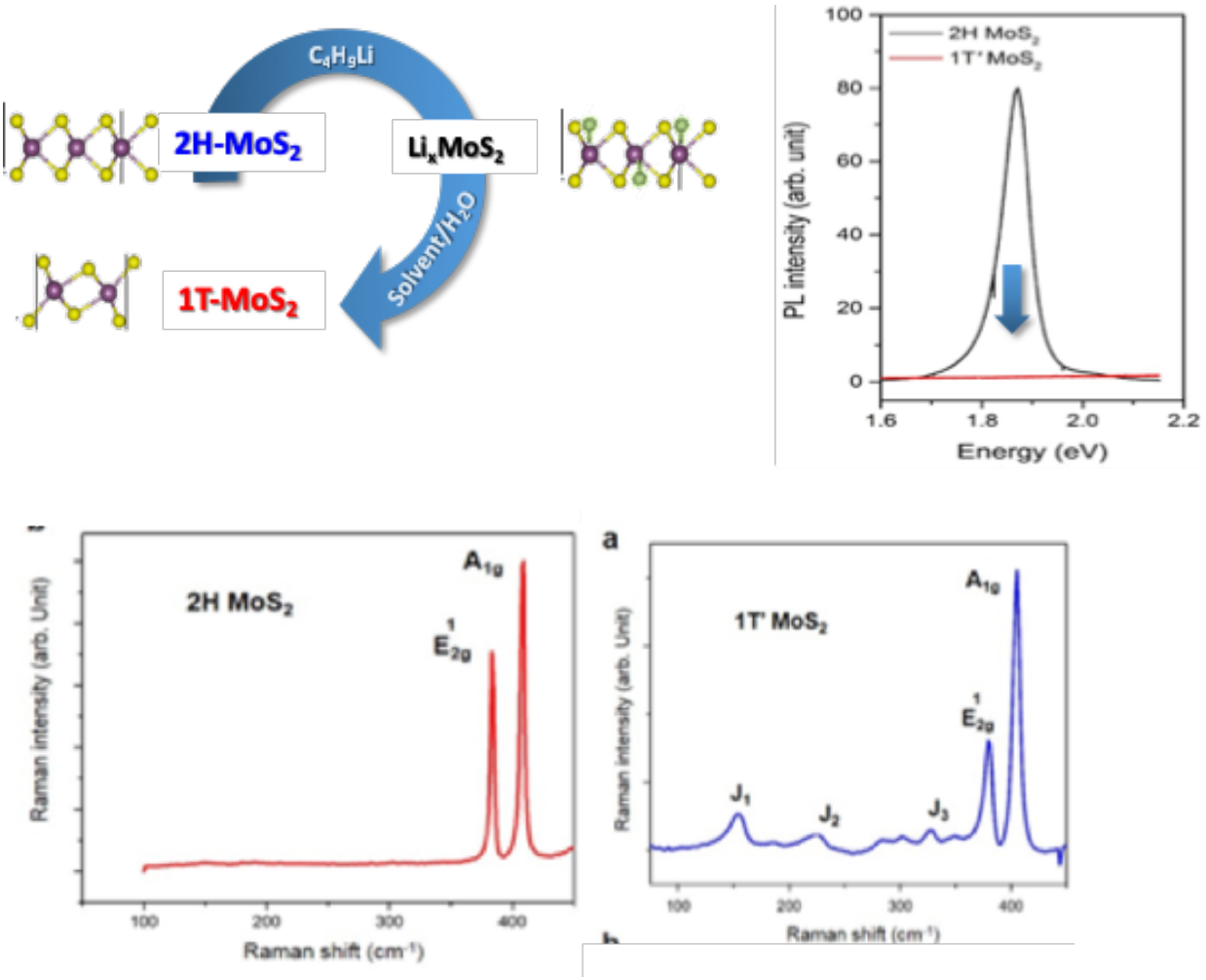


Figure 68: Schematic illustration showing phase transition of MoS_2 along with photoluminescence and Raman spectra.

A 5 min n-BuLi treatment was performed in a glovebox due to its combustible nature. This treatment leaves Li ions on the sample. The sample is then thoroughly rinsed in anhydrous Hexane to remove the Li residue. The phase transformation can be confirmed by Raman and photoluminescence spectroscopy. The Raman spectra of MoS_2 samples were measured using a Raman spectrometer (Horiba LabRAM) with a 532-nm laser with a beam spot size of ~1 μm. Figure 68 compares the Raman spectra of 1T' and 2H MoS_2.

The 2H-phase of MoS_2 exhibits two distinct Raman modes, E_{2g} at 385 cm^{-1} and A_{1g} at 405 cm^{-1}, while the 1T' MoS_2 shows additional peaks that arise from the distorted octahedral crystal structure[142]. These additional peaks are commonly known as J_1, J_2 and J_3, and are located at around 155, 225 and 335 cm^{-1}, respectively [142, 145, 146]. The presence of these three peaks confirms the phase transformation of 2H MoS_2 into 1T' MoS_2T. The PL spectra of monolayer 2H- and 1T' MoS_2 are shown in Figure 68. The 2H-phase displays a strong PL peak at 1.85 eV originating from its bandgap, while the PL of the 1T'-phase is fully quenched because of its gapless metallic nature.

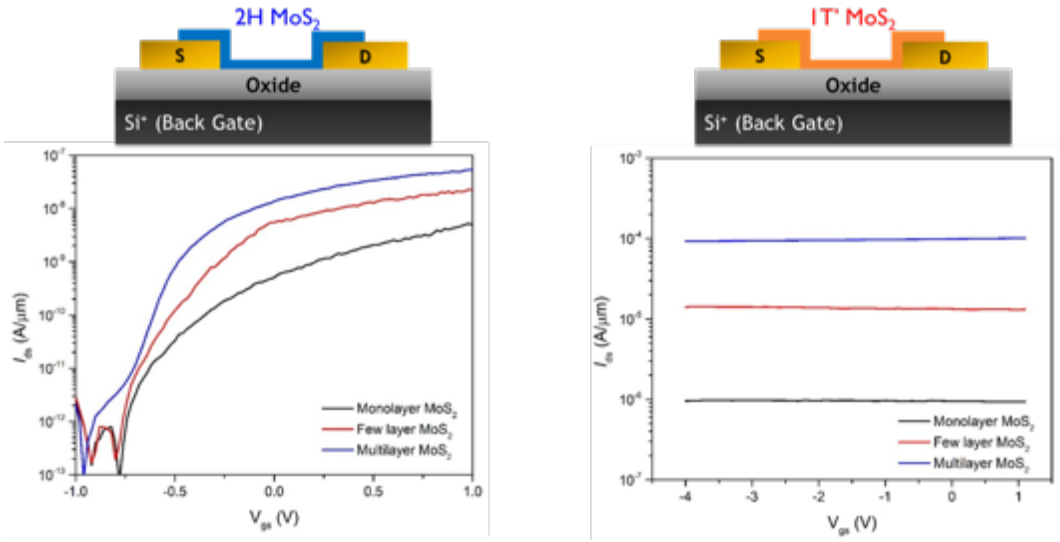


Figure 69: Transfer characteristics of backgated MoS_2 FETs for different channel thickness before and after phase transition.

To further confirm the metallic nature of the access region, backgated MoS_2FETs have been fabricated with different layer thickness on Si substrate with ALD HfO_2 gate dielectric. To ensure full phase-transformation of the MoS_2 channel, the source/drain contacts were fabricated first on the substrate and then MoS_2 flakes were transferred on top. The fabricated transistors show strong gate modulation for all thicknesses. These devices exhibit relatively higher contact resistance since the contact regions are not gated.

After initial characterization these transistors have been exposed to n-BuLi. Figure 69(b) shows the transfer characteristics of MoS_2 FET after phase-transition treatment of its channel layer. The metallic character of the 1T' MoS_2 channel prevents any current modulation by the gate electrode.

The two MoS_2 phases can, in fact, coexist by forming a stable boundary between the phases [143, 145, 147]. Selective conversion of 2H MoS_2 to 1T' MoS_2 by locally masking with PMMA and exposure to *n*-butyllithium (*n*BuLi) solution was used by Kappera *et al*. [145] to demonstrate 1T' MoS_2/2H MoS_2/metal ohmic contacts with much smaller resistance than that of the 2H MoS_2/metal contacts.

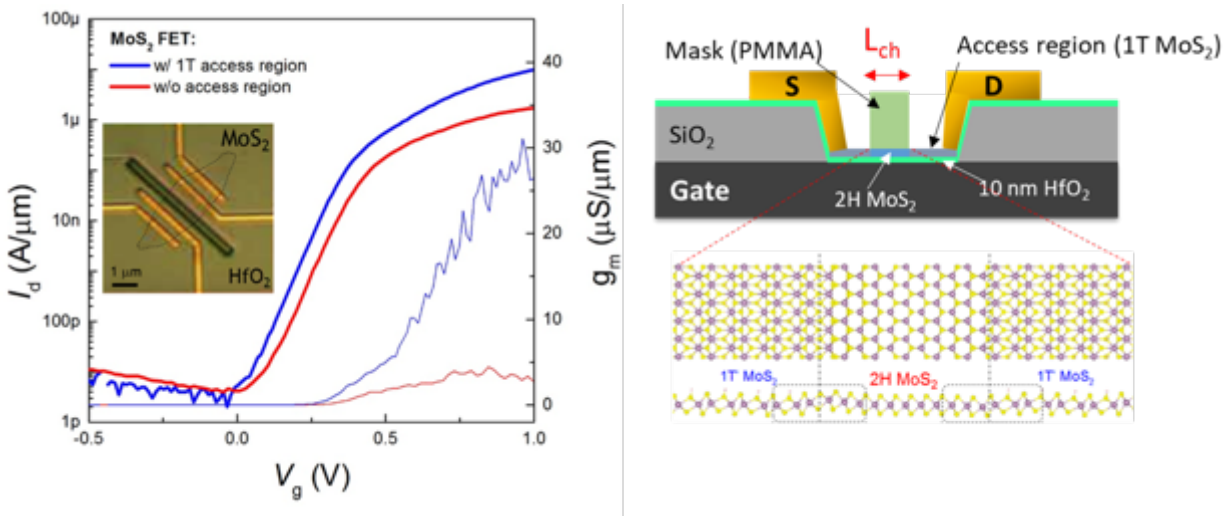


Figure 70: Transfer characteristics of 2H MoS_2 FET with 1T' access channel. Here, the channel region is defined by 400 nm wide PMMA mask.

Figure 70 shows the characteristics of backgated MoS_2 transistors with 1T' access regions, where channel has been masked using ebeam-exposed PMMA ($L_{channel}$ = 400 nm) during the n-BuLi treatment. After inducing the phase transition in the access region, both drain current and transconductance increase by 5× (1 μA/μm to 5 μA/μm and 5 μS/μm to ~25 μS/μm respectively) due to the drastic reduction of the access resistance of

the transistor. This seamless 2H/1T' MoS_2 junction has a sharp atomic interface, which reduces both the physical separation between the two materials and the tunnel barrier, and thus reducing the contact resistance [148, 149].

Unfortunately, this technology is not suitable for state-of-the-art transistors where the channel lengths are below 10 nm. Lithography is the second challenge that needs to be overcome when realizing ultra-short channel MoS_2 transistors. Electron beam lithography can potentially provide sub-10-nm patterning resolution, however it has low throughput and it is not easy to control at these dimensions. An alternative technology is directed self-assembly (DSA) of block copolymer (BCP), which has a great potential for cost-effective, nanoscale, and high-volume manufacturing. The directionality of the features in the BCP films can be defined by physical or chemical templates created by conventional lithography [150]. A few functional devices[151] have been fabricated to-date using BCP, including 29 nm pitch silicon FinFETs [152].

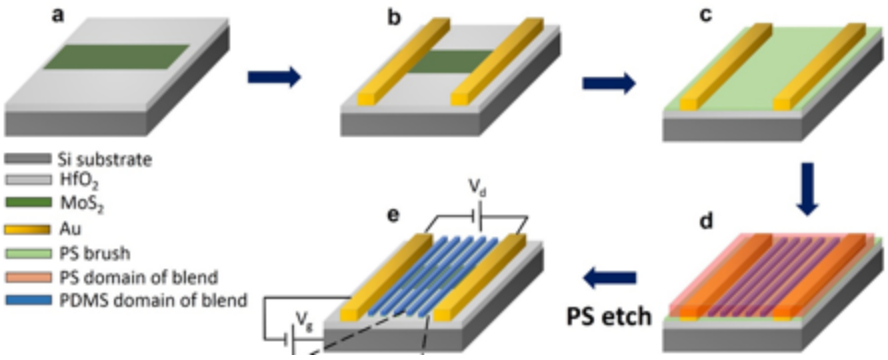


Figure 71: Key processing steps of sub-10 nm MoS_2 FET transistor fabrication process

Herein, the BCP-based technique is used for the first time to pattern a MoS_2 layer in its metallic and semiconducting phases with sub-10 nm resolution. The key processing steps are summarized in Figure 71. Each steps will be discussed in the following sections.

4.3.2 Block co-polymer self-assembly on MoS_2

To form the self-assembled BCP lines, two different poly (styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCPs were used in this work, 45.5 kg/mol (SD45; fraction of PDMS (f_{PDMS}) = 32%, period (L_0) = 43 nm) and 10.7 kg/mol (SD10; f_{PDMS} = 25%, L_0 = 15 nm). The choice of this particular BCP was dictated by its high Flory-Huggins interaction parameter, as compared to other typical BCPs, such as poly (styrene-polymethyl methacrylate) (PS-PMMA). The high Flory-Huggins interaction parameter enables lower line edge roughness and a smaller period. In addition, there is a high etch selectivity between the two blocks, PS and PDMS. Using an oxygen plasma, the organic part (PS) can be easily removed while the inorganic part (PDMS) shows high resistance to etching. First, regular MoS_2 FETs were fabricated on highly doped Si wafers coated with 10 nm of HfO_2 as the back gate stack and contacting with gold electrodes using electron-beam lithography as source/drain contacts. Next, hydroxyl-terminated polystyrene brush (PS-OH; 1.2 kg/mol, Polymer Source) was used to functionalize the surface of the substrates. PS-OH in propylene glycol monomethyl ether acetate (PGMEA) was first spin-coated on the substrate surface, which was then thermally annealed in a vacuum oven at 170 °C for 15 h, and subsequently rinsed with toluene.

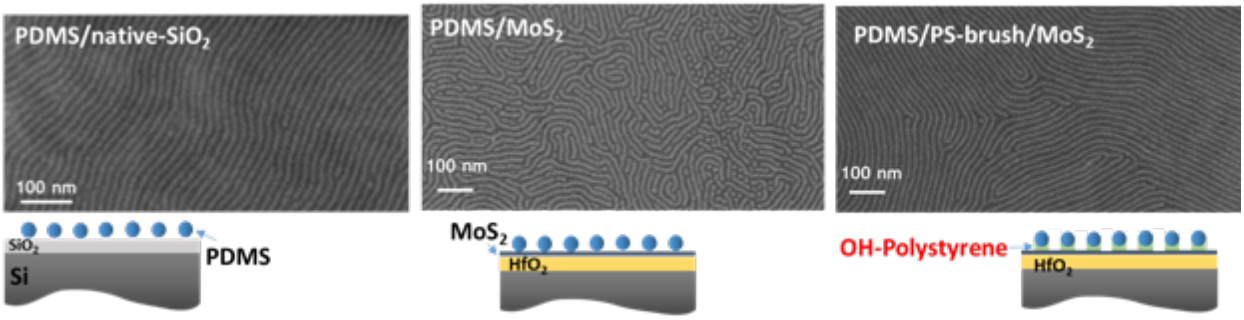


Figure 72: Poly-styrene promotes surface adhesion of PDMS on MoS_2 surface.

Next, a monolayer of PS-*b*-PDMS BCPs was spin-coated on the surface of the substrate. Two different PS-*b*-PDMS BCPs were used in the experiments: 45.5 kg/mol (SD45; fraction of PDMS (f_{PDMS}) =32%, period (L_0) =43 nm) and 10.7 kg/mol (SD10; f_{PDMS}=25%, L_0=15 nm). Then, 2 wt% SD45 was dissolved in PGMEA and 0.7 wt% SD10 was dissolved in cyclohexane for spin coating. The monolayer thicknesses of the BCPs were 29 nm for SD45 and 22 nm for SD10, and were determined by spin-coating speed. Solvent vapor annealing was performed at room temperature in a capped glass beaker. Toluene and acetone vapor was used for SD45 and SD10, respectively. This resulted in swelling of PS-*b*-PDMS BCPs, which promoted the microphase separation of the blocks. The annealing process formed periodic in-plane PDMS cylinders in the PS matrix parallel to the gold lines. Finally, CF_4 reactive ion etching was used to remove the top PDMS wetting layer followed by oxygen plasma removal of the PS matrix to leave the oxidized PDMS (ox-PDMS) patterns on the surface of the substrates parallel to the gold lines. To avoid etching of the underlying MoS_2 layer and to minimize the effect of plasma treatment on its structure, the oxygen plasma step was carried out in two parts involving direct plasma exposure for 9 s followed by placing the sample on a glass coverslip and holding it upside down 1 cm above the chuck (Figure 73). Finally, we ran a sequence of plasma pulses where the plasma power was ramped from 0 to 50 W in 3 s.

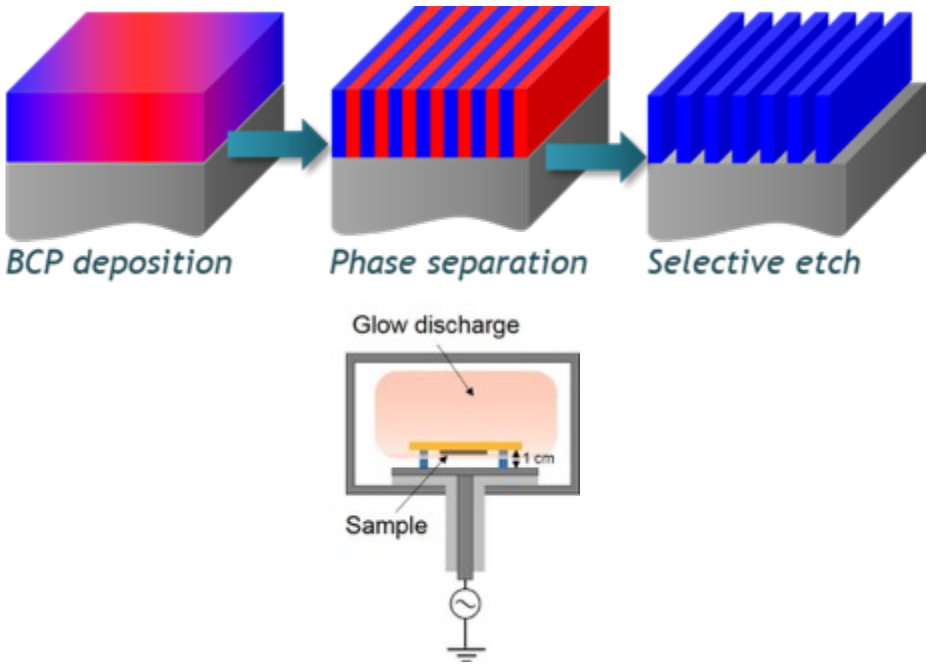


Figure 73. Fine etching of PS. Plasma setup and sample configuration used in indirect plasma PS-etching.

This indirect plasma exposure helps to markedly lower the physical effect of the oxygen radicals and to limit their reaction with the target, thus providing fine etching of PS with minimum damage to MoS_2. However, mild functionalization of the top-most layer of MoS_2 with oxygen groups still occurred.

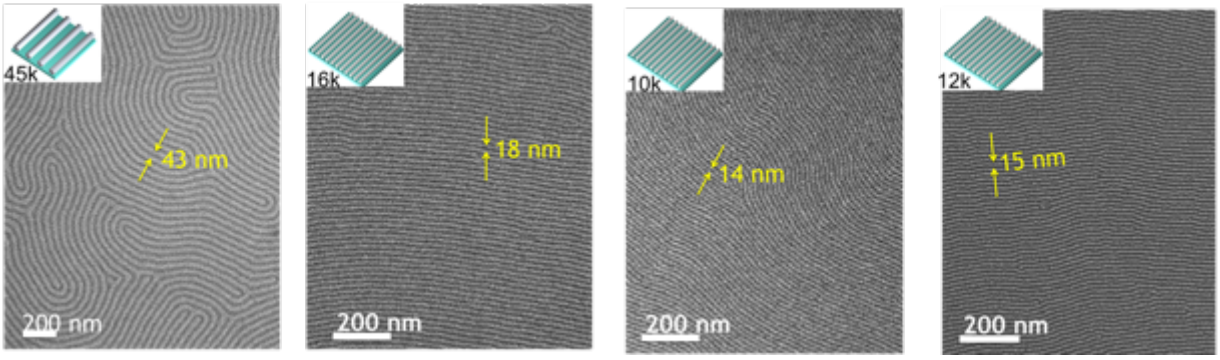


Figure 74: Block-copolymer lines with different pitch after polystyrene etch.

Without any guide the parallel polymer lines are randomly oriented on the surface. However, the presence of a guide can lead to directed-self-assembly (DSA). First, regular

MoS_2 FETs were fabricated on highly doped Si wafers coated with 10 nm of HfO_2 as the back gate stack and contacting with gold electrodes using electron-beam lithography as source/drain contacts. The channel length of these devices are designed to be integer multiple of the BCP pitch. Figure 75 top panel shows DSA of 15 nm using MoS_2 FET with channel length of 120 nm and 90 nm to achieve 6 and 8 lines respectively. Similar approach has been adopted to achieve FETs with 43 nm pitch BCP DSA.

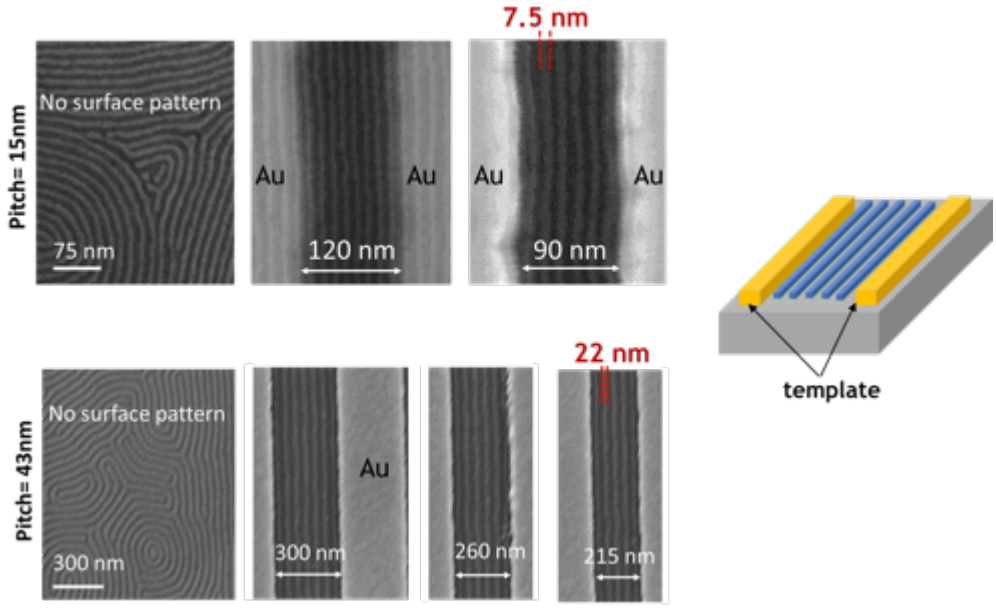


Figure 75: Directed self-assembly of BCP using source/drain of MoS_2FET as template.

In this work, the goal was to decrease the number of transistors in series by making smaller Au gaps and thus fewer PDMS lines, which define the FET channel. The metal lift-off process used here allowed us to decrease the gap to 50 nm, which can potentially provide three FETs in series. However, when the gap was below 80 nm, the orientation of the PDMS lines changed from parallel to the Au contacts to perpendicular, as shown in Figure 76. This result is similar to the results of previous work[153]. Through experiments

and simulations, it has been showed that for small gaps, when the walls of the gaps are weakly attractive to both the PS and PDMS blocks, the PDMS lines will be formed orthogonal to the walls. Therefore, the BCP self-assembly method maintains the pattern density of the lithography process. Depending on the molecular weight of the BCP and the gap between the Au lines, the number of ox-PDMS cylinders appearing between the lines varies. Although in some cases parallel orientation is achievable for smaller gap as shown in Figure 76.

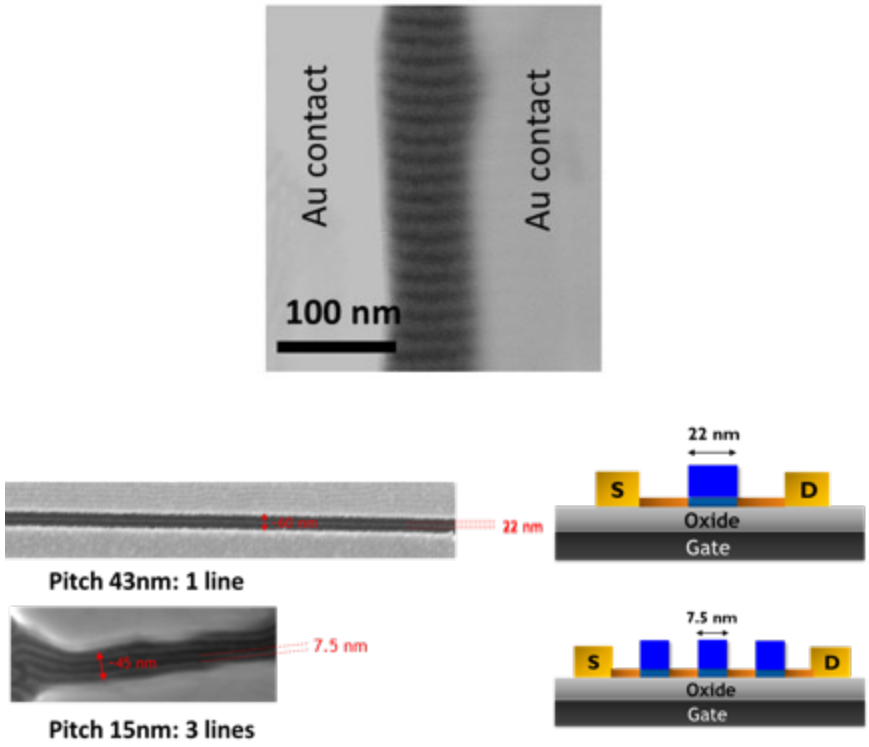


Figure 76. SEM images of a MoS_2 FET with a 60-nm gap between to its Au end contacts patterned with ox-PDMS lines showing a perpendicular configuration.

After BCP DSA and etching, the patterned MoS_2 channel was then exposed to *n*BuLi and rinsed thoroughly to selectively convert the uncovered underlying 2H MoS_2 to 1T'

MoS_2, while the BCP-covered regions remained semiconducting thus forming a chain of transistors in series where each transistor is composed of a semiconducting channel and two adjacent metallic regions forming its immediate S/D contacts. The length of each one of these three regions is anticipated to be equal to the half-pitch of the BCP lines which is either 7.5 or 22 nm, depending on the original pitch (15 nm vs 43 nm).

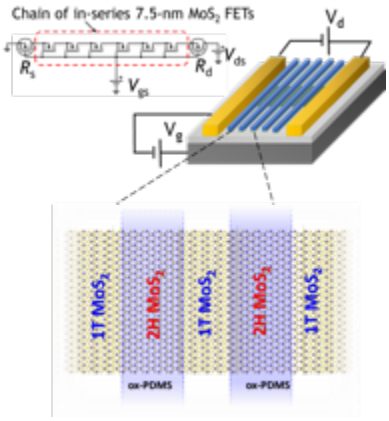


Figure 77. Fabrication of MoS_2 FETs with 7.5nm source/drain separation.

The minimum number of 7.5-nm lines formed between a pair of 90-nm-spaced Au electrodes was six, while a minimum of five 22-nm lines were formed between Au lines spaced by 215 nm.

4.3.3 Monolayer MoS_2 Transistor

In this work, exfoliated MoS_2 flakes as well as chemical vapor deposition (CVD)-grown monolayer MoS_2 were used. The CVD technique used here is compatible with advanced device fabrication technologies and can provide full substrate coverage under optimized conditions; however CVD-grown MoS_2 currently suffers from high density of structural defects. Conversely, exfoliated MoS_2 flakes have a much lower defect density but are very small in size; only tens of micrometers in diameter. MoS_2 flakes also allow

the fabrication of transistors with few-layer-thick MoS_2 channels, which can potentially stand the damage induced by plasma treatment better than monolayer CVD MoS_2 because only the topmost layer is affected by plasma treatment.

4.3.3.1 CVD growth of MoS_2

MoS_2 monolayers were fabricated by chemical vapor deposition (CVD) using the seed-promoted method[154]. Here, the precursors, molybdenum trioxide (MoO_3) and sulfur (S), were loaded in two crucibles separated in the quartz tube. A 300 nm SiO_2/Si substrate was placed face-down on the crucible loaded with MoO_3. The seeding promoter, perylene-3, 4, 9, 10-tetracarboxylic acid tetrapotassium salt (PTAS), was applied on the substrate surface. Before heating, the whole CVD system was purged with 1000 sccm Ar (99.999% purity) for 3 min. Then, 5 sccm Ar was introduced into the system as a carrier gas. The system was heated to 650 °C at a rate of 15 °C /min, and MoS_2 was synthesized at 650 °C for 3 min under atmospheric pressure. The temperature at the position where the sulfur was located was set to be around 180 °C during growth. The system was finally quickly cooled down to room temperature by opening the furnace and taking out the quartz tube, and 1000 sccm Ar flow was used to remove the reactants. With the assistance of the seeding promoter, continuous monolayer MoS_2 film with triangle domain shapes were synthesized on the substrate. Figure 78(b) shows SiO_2/Si substrates with different coverages of MoS_2 ranging from isolated triangular single crystal MoS_2 to full coverage.

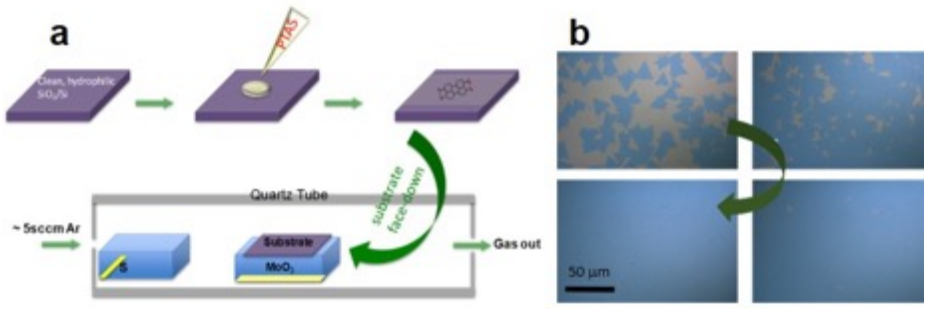


Figure 78. CVD growth of MoS_2. (a) Schematic illustration of CVD setup for monolayer MoS_2 growth. (b) Optical images of monolayer MoS_2 films on SiO_2/Si substrate at different coverage stages.

4.3.3.2 Transport characteristics of monolayer-MoS_2 FET

Figure 79 (a) shows the evolution in the transfer characteristics (I_{ds}-V_{gs}) from a 120 nm monolayer MoS_2 FET (ML-MoS_2 FET) to a patterned 2H/1T' ML-MoS_2 FET with a half-pitch of 7.5 nm.

As can be seen in Figure 79(a), the ML-MoS_2 has survived the PS etching step and still shows high I_{on}/I_{off} modulation. However, current degradation of more than two orders of magnitude is observed as well as a worse SS and shifted subthreshold voltage (V_t) compared with the as-fabricated MoS_2-FET. These changes are the consequences of the MoS_2 surface being affected by the plasma radicals. The unwanted degradation is nevertheless a direct indication that the PS film is fully etched and the gap between ox-PDMS lines is fully opened and ready for *n*BuLi treatment. We need to consider that a monolayer of MoS_2, used in the device of Figure 79, is the extreme case in this etching

process, and obviously a thicker MoS_2 channel would be less affected by the process as the underlying layers would be shielded against the radicals by the topmost layer.

The last I_{ds}-V_{gs} curve in Figure 79(a) shows the same device characteristics after *n*BuLi treatment. Since 1T' regions are fully metallic, they play a role as contacts to the semiconducting 2H regions under the ox-PDMS cylinders. This configuration effectively presents a chain of transistors in the series mode where each one has a 7.5-nm 2H-MoS_2 channel, seamlessly contacted to 7.5-nm-long 1T'-MoS_2 on both sides as S/D contacts, as shown schematically. The pronounced changes are the increase in current and further degradation of SS. The former change arises from the semiconducting to metallic conversion that decreases the effective channel length and the latter change results from the so-called short channel effect, which will be discussed in detail later in this work. This chain of transistors demonstrates the operation of MoS_2 transistors with the shortest and thinnest channel, that is ~7.5 nm long and ~7 Å thick, reported to date. Figure 79(b) shows the final device at different V_{ds} values highlighting the increase of I_{off} at V_{ds}=1 V, which can be attributed to direct source-drain tunneling. This matter in discussed in more detail in the section 4.4.

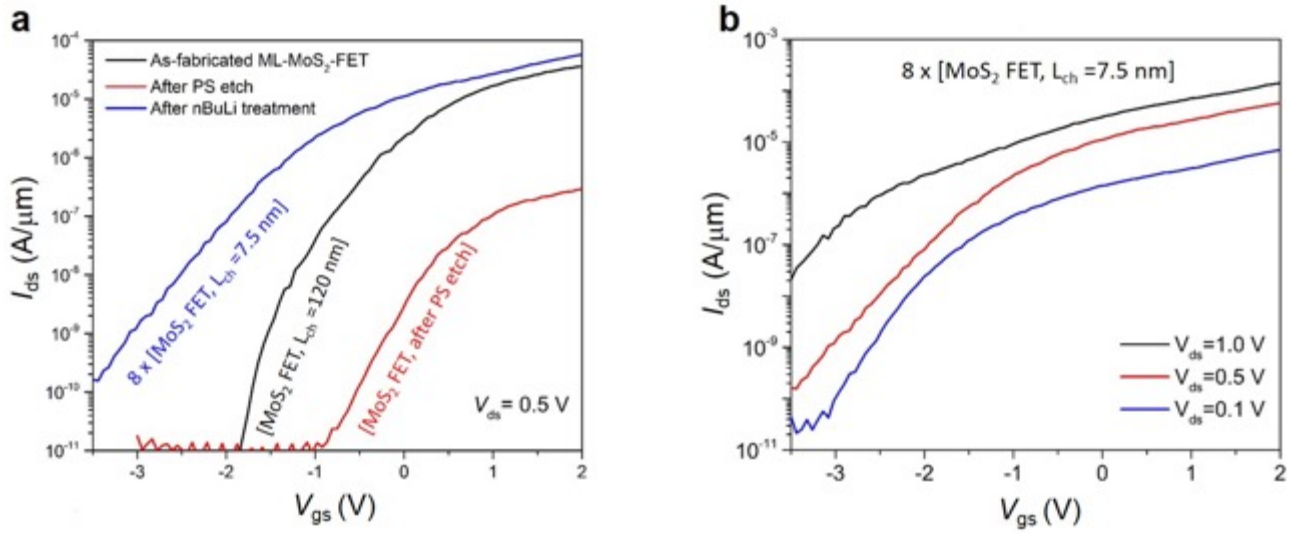


Figure 79. Characterization of 7.5-nm ML-MoS_2 FETs. (a) Evolution of a CVD monolayer MoS_2-FET showing I_{ds}-V_{gs} characteristics at V_{ds} = 0.5 V of the as-fabricated (channel length=120 nm), after PS-etch and after phase transition treatment with nBuLi. The phase transition treatment converts the long channel to a chain of short channel transistors in series with a channel length of 7.5 nm connected together with a metallic 1T' MoS_2 junction. (b) I_{ds}-V_{gs} of the final device at different V_{ds} values.

We also tested BCP with a pitch of 43 nm, which provides transistor channels with a nominal length of ~22 nm. Figure 80 compares the transfer and output characteristics of a monolayer MoS_2 device with 215-nm channel length before and after patterning into a chain of five 2H/1T' MoS_2 regions. Similar to the chain of the 7.5-nm MoS_2 FETs, both larger on-current and off-currents are observed along with increased SS. The I_{ds}-V_{ds} curve of the as-fabricated ML-MoS_2 FET shows excellent current saturation, which is distorted after formation of short-channel transistors.

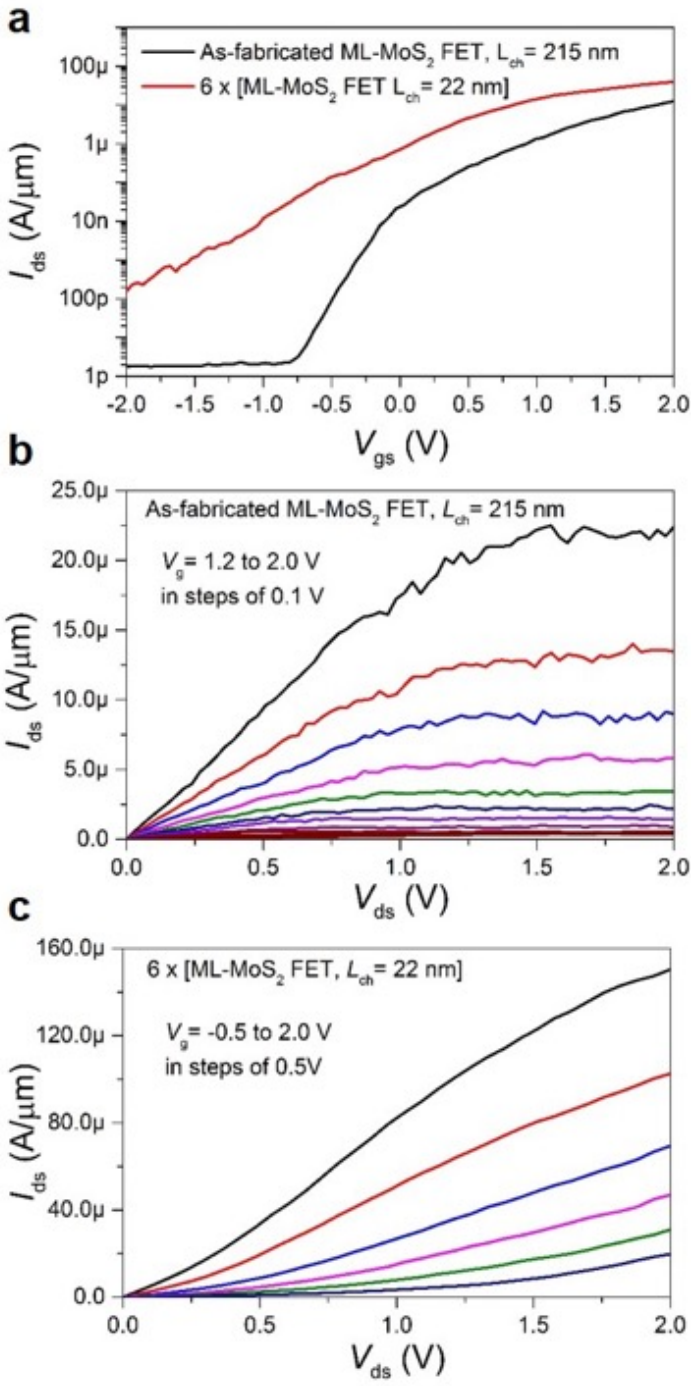


Figure 80. Characterization of 22-nm ML-MoS_2 FETs. (a) I_{ds}-V_{gs} characteristics of an as-fabricated 215-nm monolayer MoS_2 device and final device with six 22-nm channels in series. (b) and (c) I_{ds}-V_{ds} characteristics of the as-fabricated and final device, respectively.

4.3.4 Transport characteristics of Tri-layer MoS_2 Transistor

In this section, we will discuss the experimental performance of a device with 7.5-nm channel length constructed on exfoliated trilayer MoS_2, which exhibits the best performance and shortest channel length among the fabricated devices. We use a highly doped Si substrates with a 10 nm of HfO_2 layer on the surface as the back-gate stacks for all devices in the current study.

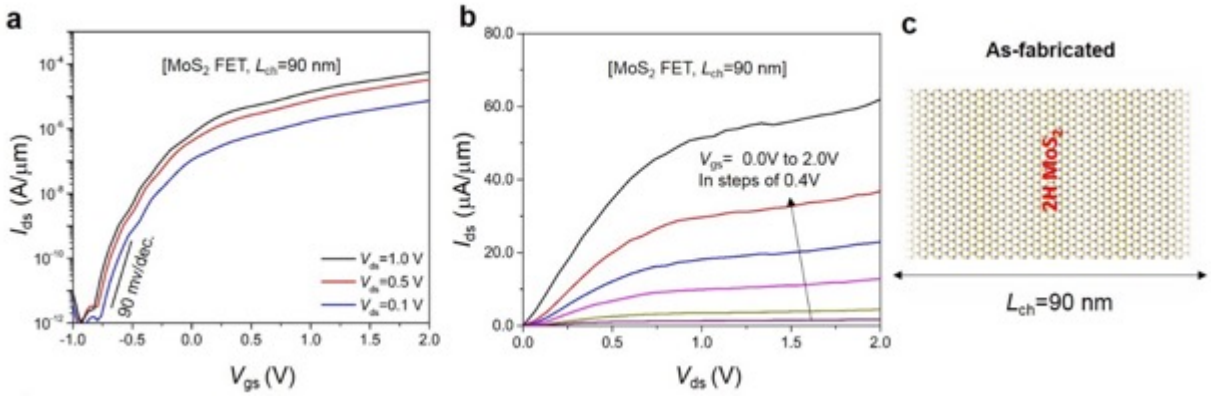


Figure 81. (a) and (b) I_{ds}–V_{gs} and I_{ds}–V_{ds} of an as-fabricated trilayer MoS_2 FET with channel length of 90 nm and EOT of 4 nm. (c) shows schematic of 2H MoS_2 channel.

Figure 81 shows I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics of a trilayer MoS_2 FET before phase transition of access regions. The as-fabricated device with channel length of 90 nm shows good subthreshold characteristics with small DIBL< 0.1V/V, SS = 88 mV/dec and current saturation in I_{ds}-V_{ds} characteristics owing to velocity saturation. After initial characterization BCP DSA has been performed on the device and it exhibits similar degradation behavior due to plasma damage. However, the extent of the degradation is much smaller due to tri-layer nature of the channel.

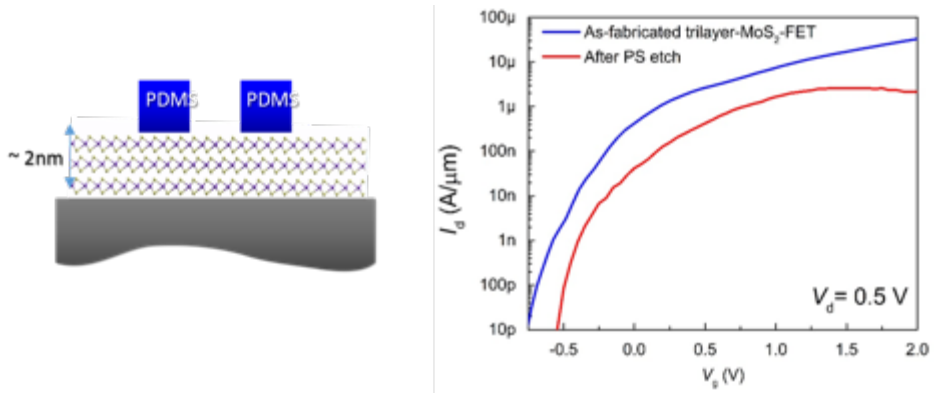


Figure 82. Schematic and transfer characteristics of trilayer MoS_2 FET before and after PS etch.

The chain of in-series 7.5-nm MoS_2 FETs, formed after the *n*BuLi treatment shows a well-defined I_{ds}-V_{gs} performance with an I_{on}/I_{off} ratio in excess of 10^7 with SS_{min} of 120 mV/dec and I_{on} of 0.25 mA μm at V_{ds} = 1 V. Thanks to the extremely thin body thickness and the wide bandgap of the MoS_2 channel, the short channel length of this device has a minimum impact on its subthreshold characteristics and the off-state current, I_{off} < 10 pA/μm. However, compared with the I_{ds}-V_{gs} characteristics of the long channel, the device shows larger DIBL of ~ 0.7 V/V. This also leads to the absence of saturation in the I_{ds}-V_{ds} curves despite the high current density in the mA/μm range, which is rather high for MoS_2 transistors. These characteristics are further explored using device modeling in the discussion that follows.

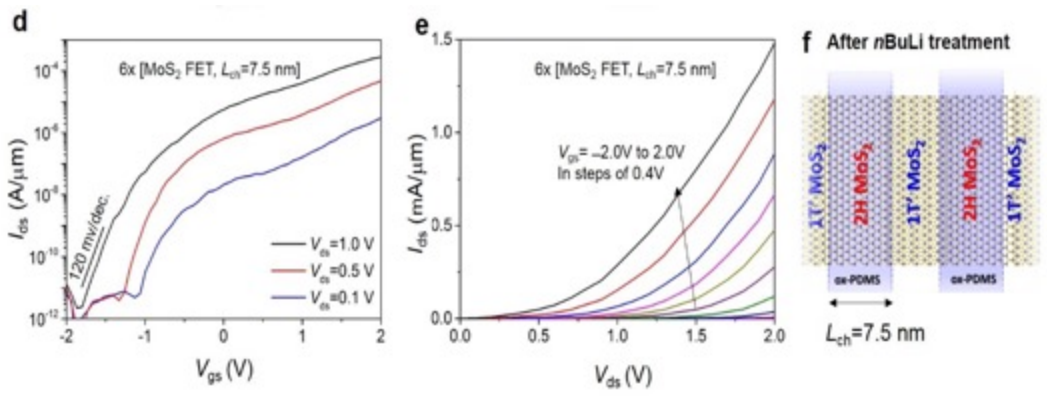


Figure 83. (a) and (b) I_{ds}–V_{gs} and I_{ds}–V_{ds} of the same set of I-V curves shown in Figure 81for the chain of six 7.5-nm MoS_2 in-series FETs produced after a phase transition treatment with nBuLi.

4.4 Theoretical analysis of the device characteristics

To further analyze the performance of the sub-10-nm MoS_2 channels, the MIT Virtual Source Compact model (MVS)[155] was use to fit the experimental data for the MoS_2 FETs. The parameters from the MVS model have been used as predictive transport modeling using Non-equilibrium Green's function approach. Moreover, density functional theory was also used to understand the nature of 1T/2H MoS_2 junction.

4.4.1 MIT Virtual Source model: Application to ultra-scaled MoS_2 FET

In the past, the MVS model has been applied to short channel silicon[155], III-V semiconductors[156-158], GaN and graphene[159] to extract device parameters such as injection velocity, carrier mobility, and access resistance (which is equivalent to the 2H/1T' junction resistance in this work). Here, gate capacitance, channel length, DIBL and subthreshold swing are directly determined from the experimental data while the remaining parameters (carrier mobility and velocity) are extracted by best-fitting the full

I-V data. The MVS model adopts the VS-concept of carrier-injection pertinent for quasi-ballistic transport in scaled gate-lengths (L_g) where channel-current (I_{DS}) is computed at the VS-point (x_o) as [160]:

$$I_{ds} = Q_{xo} v_{xo} F_{sat}$$

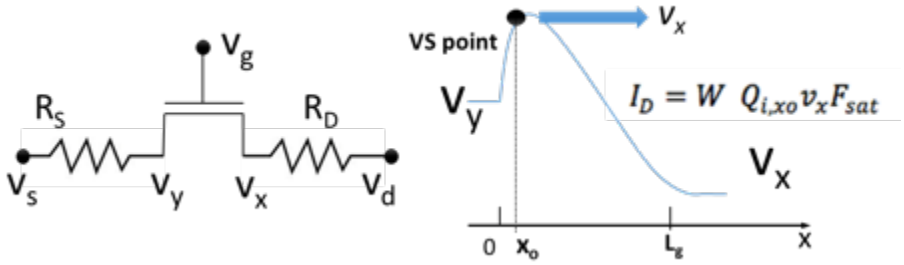


Figure 84. The concept of virtual source injection modeling

where Q_{xo} is the charge density at the top of the channel barrier, located at the virtual source (VS) or the injection point near the source contact. v_{xo} is the injection velocity (at the VS point) and V_{ds} is the internal applied voltage excluding the voltage drops in the access resistances R_s and R_d. F_{sat} is an empirical function that captures the saturation of the drain current with drain bias.

$$F_{sat} = \frac{V_{ds}'}{V_{DSAT}} \Big/ \left(1 + \left(\frac{V_{ds}'}{V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}$$

which gradually varies from 0 to 1 as the drain bias is changed from 0 to V_{DSAT} and β is an empirical (typically around 1.4-1.8) parameter to match the shape of the output characteristics.

$$Q_{x0} = C_g n\phi_t ln\left(1 + exp\left(\frac{(V_G - V_{Si}) - (V_T - \alpha\phi_t F_{f,})}{n\phi_t}\right)\right)$$

Q_{xo} is a primarily determined by the gate voltage V_{gs} and to some extent by the drain bias V_D through a drain induced barrier lowering (DIBL) term, δ. Gate capacitance, C_{ox}, the subthreshold swing parameter n and the threshold voltage parameter V_t decides the shape and transition (from exponential to linear) points of Q_{xo}. The channel charge is self-consistently partitioned based on energy conservation and current-continuity [161] as follows (where γ is the ballistic factor, m_0^* is effective carrier-mass),

$$Q_{S,Ch} = WL_g Q_i(x_0)\left[\frac{\sinh^{-1}(\sqrt{k})}{\sqrt{k}} - \frac{\sqrt{k+1}-1}{k}\right]$$

$$Q_{D,Ch} = WL_g Q_i(x_0)\left[\frac{\sqrt{k+1}-1}{k}\right];\ k = \frac{2qV_{DSi}}{\gamma m_0^* v_{xo}^2}$$

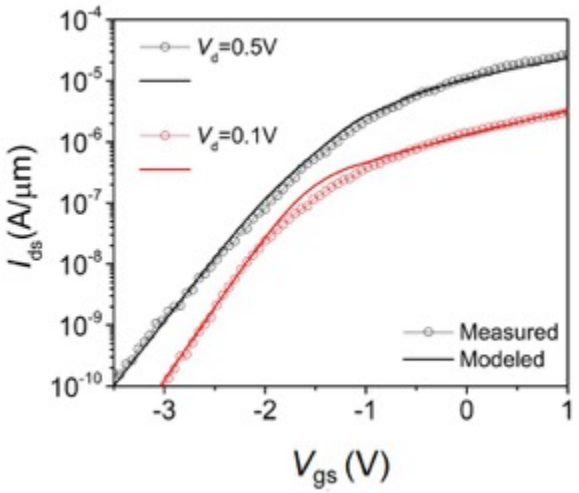


Figure 85. MVS fit of monolayer device transfer characteristics. I_{ds} vs V_{gs} characteristics of fabricated MoS_2 FET at different V_{ds} along with MVS fitting of the characteristics.

Figure 85 shows the MVS fitting for the monolayer device. The monolayer devices have a larger DIBL of 0.75 V/V and higher SS (~460 mV/dec.) than their trilayer counterparts, which have a DIBL of 0.7 V/V and SS of 120 mV/dec. These discrepancies

can be attributed to a lack of plasma-induced defect states in the channels of the tri-layer MoS_2 devices. The other parameters are mobility μ=12 cm^2/V.s, resistance R=80 $\Omega.\mu m$ and velocity v_{xo}=of 8×10^5 cm/s.

The circuit used in the Advanced Device Simulator (ADS) is shown in Figure 86. In addition to the chain of transistors, two extra transistors (circular blocks) are used with

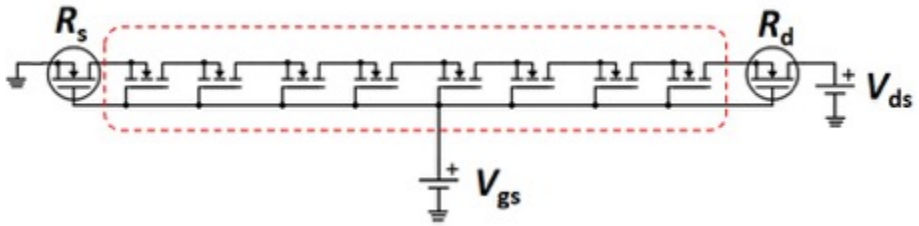


Figure 86. Circuit configuration used in ADS. Circuit configuration of the series of FETs used in ADS simulator and corresponding biasing configuration.

similar MVS parameters to represent V_{gs} dependent R_s and R_d. R_s and R_d are representing the gate voltage dependent contact resistances.

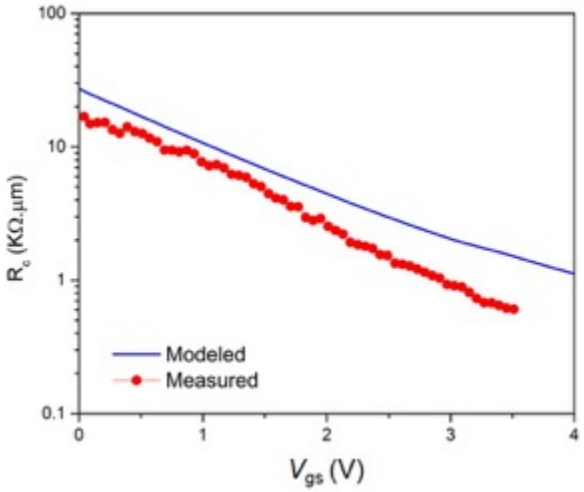


Figure 87. Contact resistance modeling. Contact resistance vs. gate voltage from the model and experimental data.

Figure 87 shows the contact resistance used to fit the data. The MoS_2 sample has low carrier density at V_{gs}=0, yielding a contact resistance ~20 KΩ.μm. The contact resistance decreases below 1 KΩ.μm when the channel is sufficiently populated with carriers. The total contact resistance (blue line) that fits the experimental transfer curve is close to the contact resistance of our MoS_2 device shown in red circles

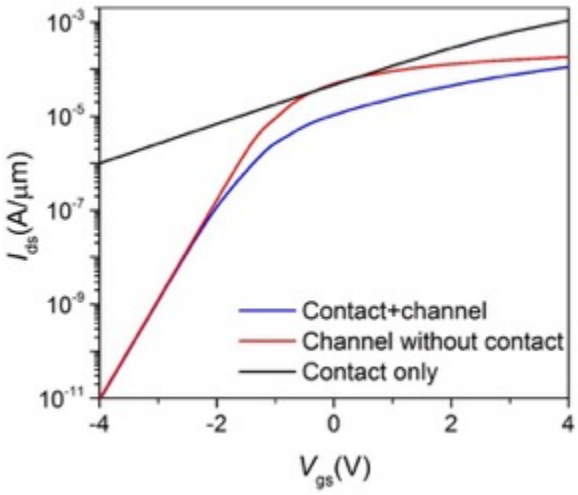


Figure 88. Effect of contact resistance. Transfer characteristics of the monolayer device with and without the contact resistance.

Figure 88 shows the effect of the contact resistance on the transfer characteristics. With the contact resistance, the output current increases slowly above threshold and takes a much higher voltage (blue) to saturate than it takes without the contact resistance (red). The black line shows the current if only the contact were considered in the circuit. Below threshold the current changes exponentially and the transport is controlled by the MoS_2 transistors. But above the threshold ($V_{gs} > -1$ V); the current changes in a superlinear fashion, which results from the contact resistance. At higher voltages (V_{gs}>1V), channel resistance dominates again.

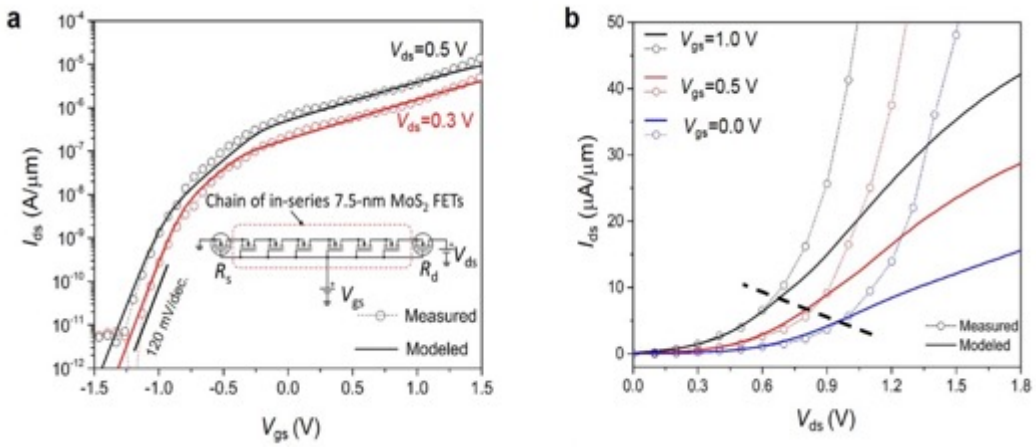


Figure 89. (a) and (b) MVS fit of the transfer and output characteristics. I_{ds}–V_{ds} fits the model well for V_{ds} <0.6 V. At higher voltages, the direct source-to-drain tunneling becomes substantial. The dashed line in (b) is intended as a visual guide to indicate the two regimes. The inset in (a) shows the circuit configuration used in the MVS model consisting of a chain of six 7.5 nm MoS_2 FETs and V_{gs}-dependent R_s and R_d.

The similar analysis has been performed on the tri-layer device. Figure 89 (a, b) compares the experimental transfer and output characteristics of the trilayer MoS_2 chain of in-series FETs with the model fitting. The parameters of the contact-modeling transistors were used purely as fitting parameters here; however, the resulting contact resistance and its gate voltage dependence are well matched with the experimental Au-MoS_2 contact resistance data extracted in this work as discussed in the previous section. The injection velocity (v_{xo}) and the mobility are found to be ~1×10^6 cm/s and 25 $cm^2/V\cdot s$, respectively, and the access resistance (where $r_s = r_d = r_{2H/1T'}$) is as low as 75 Ω·□m, which indicates the ohmic nature of the 2H/1T' junction; this aspect will be further discussed later in this work. The device also has a very low I_{off} (<10 pA/□m) and high I_{on}/I_{off} ratio, in good agreement with previous theoretical expectations [162, 163]. This is a result of the ability of MoS_2 to suppress direct source-drain tunneling thanks to its high effective mass.

The lack of saturation in the I_{ds}-V_{ds} characteristics and the deviation of the current from the MVS model (for $V_{ds} > 0.6$ V), as indicated in Figure 89(b), is mainly because of

large DIBL induced by the relatively large effective oxide thickness (EOT) used in this work (~4 nm, vs ~0.8 nm in state-of-the-art CMOS technology). To clarify this point, we perform quantum mechanical simulations using non-equilibrium Green's function (NEGF) formalism for a single 7.5-nm MoS_2 FET.

In the NEGF model used in this work the 2D Poisson equation is converted into a 1D equation[134]

$$\frac{d^2\psi}{dx^2} - \frac{\psi - \phi_{gs}}{\lambda^2} = -\frac{\rho}{\epsilon}$$

provided that the effective scaling length is $\lambda = \frac{\sqrt{t_{ox} t_{semi} \epsilon_{2D}}}{\epsilon_{ox}}$. ψ is the surface potential and $\phi_{gs} = V_G - V_{FB}$ is the gate potential. Charge density at each point is calculated from the non-equilibrium Greens function (NEGF) formalism[164],

$$\rho = \frac{q}{2\pi} \int_{E_c}^{\infty} [G\Gamma_S G\, f_S + G\Gamma_D G\, f_D] dE$$

where f_s and f_d are the source and drain Fermi Functions. G is the retarded Green's function calculated at an energy E from,

$$G = (E\mathbf{I} - H + \psi - \Sigma_s - \Sigma_D)^{-1}$$

A single band effective mass Hamiltonian is used from the discretized Schrodinger equation. Effective mass and bandgap parameters are taken from Alam *et al*.[165] Source to channel barrier height is set to $E_g/2$ when $V_{gs} = 0$. The contact self-energy matrices calculated from contact surface Green's function, $g_s = \left(\left(E + \phi_{0,L}\right)I - H - \tau^+ g_s \tau\right)^{-1}$ which is solved iteratively. ϕ_0 and ϕ_L are the boundary potentials for the particular barrier height and drain bias. In order to capture the 2D density of states, a transverse k_y dependent Hamiltonian is used. Transmission and density of states are found by inverse

Fourier transforming to the real space[166]. Inversion of the matrices are expedited by using Recursive Green's function Algorithm[167]. The self-energy matrix is found from $\Sigma = \tau^{+} g_s \tau$ and the anti-Hermitian components give the broadening matrixΓ. Once the self-consistency is achieved between ρ andψ, current is calculated from

$$I = \frac{2q^2}{h} \int Tr[G\Gamma_s G\Gamma_D](f_s - f_d)dE$$

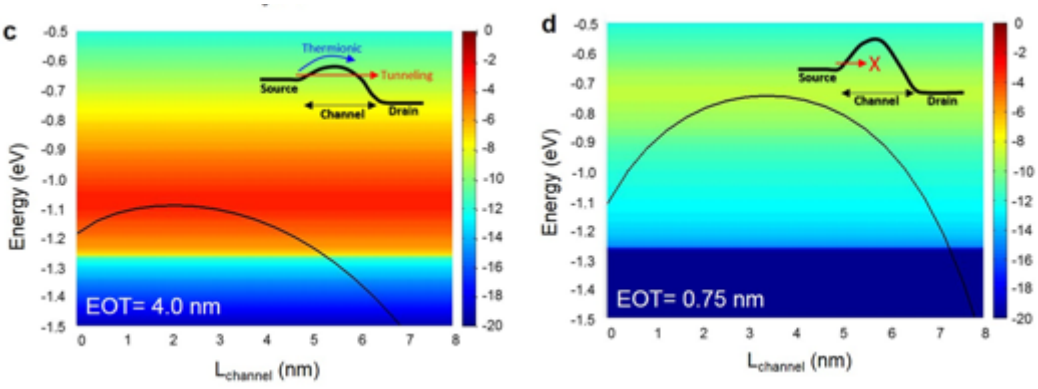


Figure 90. (a) Energy-resolved total transmission probability T (scale is in $\log_{10}(T)$ and T is in units of nm^{-1}) from NEGF simulation for EOT of 4 nm, showing substantial tunneling through the barrier in the off state with high drain bias of V_{ds} = 0.6 V. (b) T for EOT of 0.75 nm, where the tunneling current this time is suppressed by orders of magnitude. Insets in (a) and (b) schematically illustrate the tunneling and thermal emission currents

For the thicker oxide (4-nm EOT, Figure 90 (a)), the barrier at the off-state (V_{gs}=0) with high drain bias (V_{ds}=0.6 V) is low enough to cause both high thermal emission currents and direct source-drain tunneling. This is in good agreement with the experiments, however it should be noted that as the experimental device has six transistors in series, it takes roughly six times the voltage drop across one transistor to

produce the same level of tunneling current predicted by the simulation. It should be noted that for low V_{ds} values (up to ~0.6 V), the tunneling contribution is negligible (less than 10%) and the transport is determined by thermal emission.

NEGF simulations of a thinner oxide (0.75-nm EOT) predict a significant reduction in the transmission probability of at least five orders of magnitude both below and above the barrier. This is because the barrier height is now higher and the potential reaches the peak much more quickly thanks to the lower scaling length. The effective mass of MoS_2 is large enough to reduce DIBL for the 0.75-nm EOT to approximately 72 mV/V and the subthreshold slope to about 73 mV/dec, as shown below.

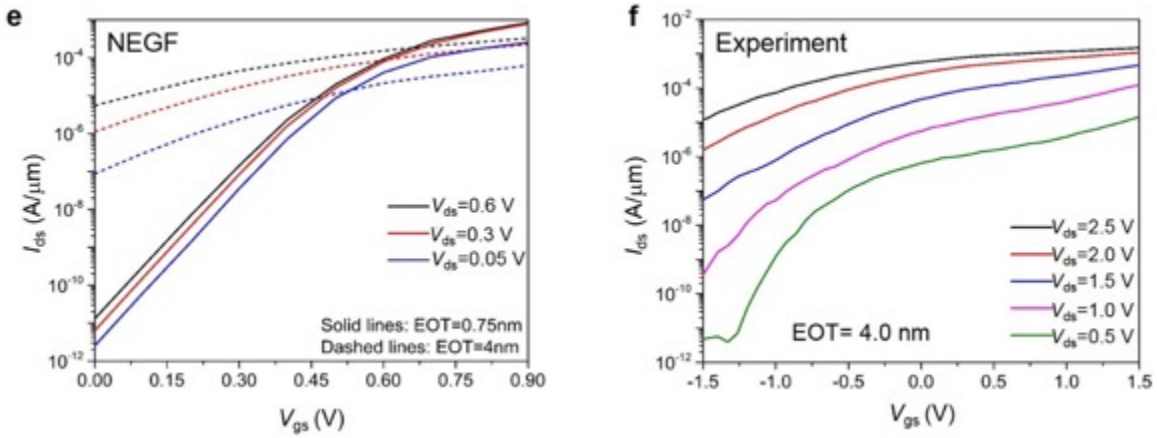


Figure 91. (a) Transfer characteristics from NEGF for two different EOTs, showing significantly improved subthreshold slope and DIBL for the EOT of 0.75 nm. (b) Experimental I_{ds}-V_{gs} curves of the chain of 7.5-nm MoS_2 FETs at different values of V_{ds} showing substantial increase of I_{off} with increasing V_{ds}, in agreement with the modeling in (a).

After developing a good understanding of the chain in-series FETs, NEGF model can be used to predict a single transistor with scaled EOT. Figure 92(g) and (h) show the MVS-calculated transfer and output characteristics of a single 7.5-nm MoS_2 transistor, as

modeled using the DIBL and subthreshold slope parameters extracted from the NEGF simulation with a 0.75-nm EOT and Vt=0.5 V (Figure 90(a)). In these simulations, the velocity, mobility and resistance ($r_{2H/1T'}$=75 Ω·μm) were taken from the MVS fit of the trilayer device. The device shows an I_{on}/I_{off} in excess of 10^6 with I_{off} as low as ~100 pA/μm and I_{on} of ~230 μA/μm at

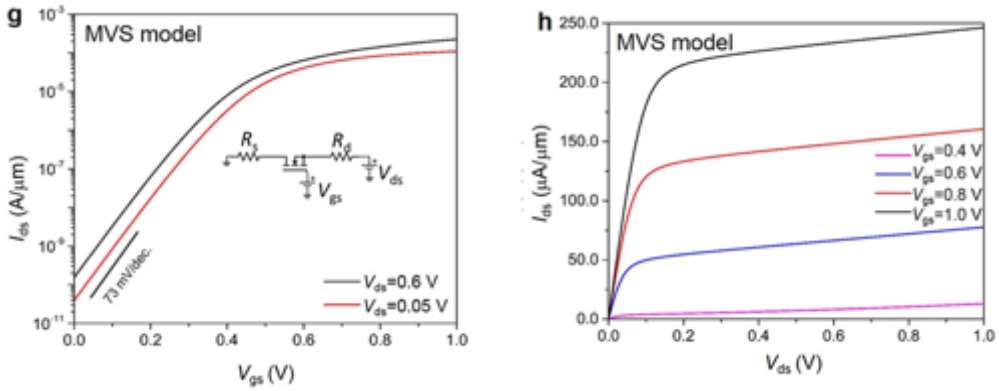


Figure 92. (a) and (b) MVS prediction of transfer and output characteristics, taking into account the mobility, injection velocity and resistance found in (a), (b). EOT of 0.75 nm is used. DIBL (72 mV/V) and subthreshold slope (~73 mV/dec.) are taken from (a). V_{gs}=0.6 V. These numbers are not far from the requirements envisaged in the International Technology Roadmap for Semiconductors (ITRS)[168] for the 2024 low-power devices node (L_g = 7.5 nm, I_{on} = 400 μA/μm, I_{off} = 10 pA/μm). Further improvements in both the contact resistance and the on current are required however, which may be made possible by the development of better MoS_2 growth techniques.

4.4.2 Density Functional Theory analysis of the 2H/1T MoS_2 junction

To understand the origin of lower contact resistance by phase transformation of the access region, two important points about the 2H/1T' junction must be addressed. The first is the stability of the 1T' phase and the stability of its junction with the 2H phase,

and the second is the formation of an ohmic interface, *i.e.*, a low barrier contact between the two phases that allows the 1T' regions to act as suitable source or drain contacts to the 2H MoS_2 channel. Because MoS_2 FETs are *n*-type, these contacts must have a low work function to form effective ohmic contacts. To determine whether or not the 2H/1T' MoS_2 junctions fulfill these requirements, DFT calculations of the 2H MoS_2 phase and of both pristine and functionalized 1T' phases and their junctions have been performed.

DFT calculations were performed using the Vienna *ab initio* simulation package[169] with projector-augmented wave potentials[170, 171]. The generalized gradient approximation parameterized by the Perdew–Burke–Ernzerhof functional [172] was used as the exchange-correlation functional. The lattice constants of monolayer 1T'- and 2H-phase MoS_2 were obtained *via* structural optimization. The lattice mismatch between the two phases in constructing the 2H/1T' lateral junction was smaller than 0.05%. The vacuum layers were more than 20 Å thick to ensure decoupling between neighboring slabs. The energy cutoff was 450 eV for the plane-wave basis sets. During structural relaxation, all the atoms were allowed to relax until the force on each atom became smaller than 0.02 eV/Å. A Gamma-centered 9×15×1 k-point mesh was used for the $\left(1 \times \sqrt{3}\right)$ cell and one of 1×15×1 was used for the 2H/1T' junction. The adsorption site and configuration of H were carefully examined, and all the calculations were spin-polarized.

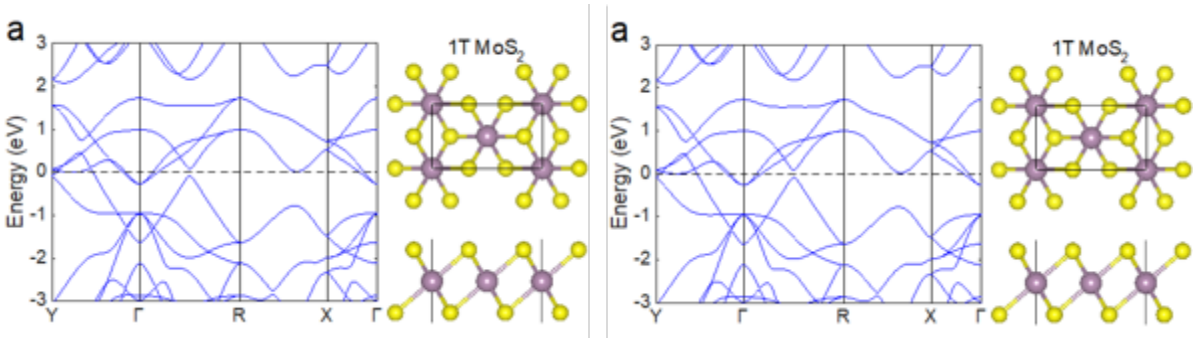


Figure 93. Electronic band structures and atomic structures of 1T (a) and 1T' (b) MoS_2.

Figure 94 compares the electronic and atomic structures of 1T and 1T' MoS_2. The 1T' phase is more stable than 1T by 0.29 eV per formula unit, and both phases are calculated to be metallic.

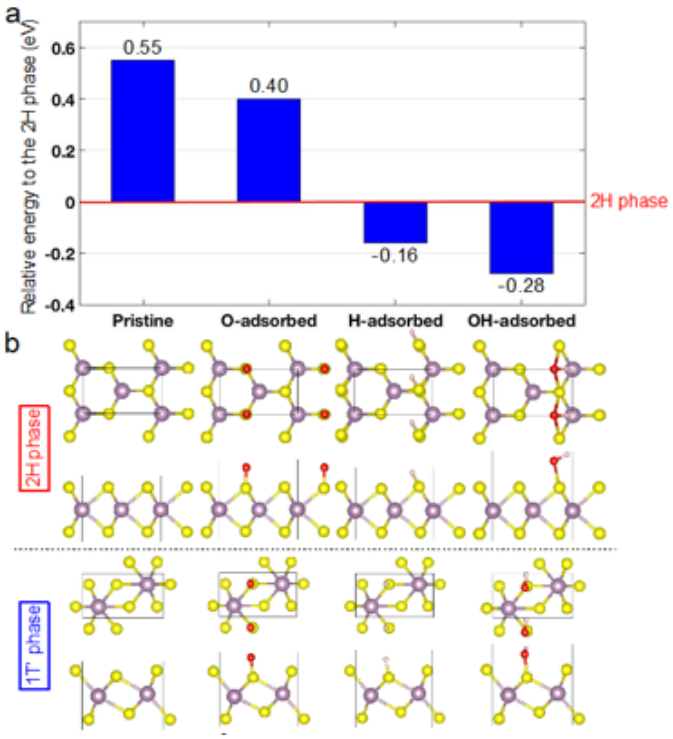


Figure 94. (a) The energy per formula unit of the 1T' phase with respect to the 2H phase. Energies of the pristine, O-adsorbed, H-adsorbed, and OH-adsorbed 2H phases are all set to zero as the reference. The negative values mean the 1T' phase is more stable. (b) Top and side views of the atomic structures of the pristine and functionalized 2H and 1T' phases.

Although the 1T' phase is less stable than the 2H phase in the pristine form, as shown in Figure 94, it becomes even more stable with the addition of H or OH. However a small bandgap (E_g < 400 meV) opens up in the electronic structures of the functionalized 1T' MoS_2. Nevertheless, the 1T' phase retains its metallic characteristics upon the adsorption of H or OH groups as the Fermi level is well above the conduction band edge.

The pristine 1T' phase has a high work function of 5.8 eV when compared with the electron affinity of 2H MoS_2, which is ~4.3 eV as shown in Figure 95 (a) and (b). Such a large energy difference would form a significantly high Schottky barrier for both MoS_2 thicknesses and would

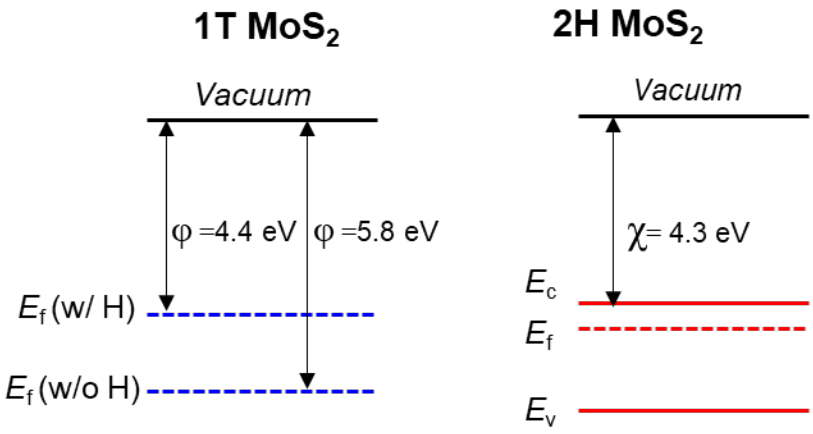


Figure 95. (a) Band diagram of 2H MoS_2. The calculated electron affinity value is χ= 4.3 eV. (b) Calculated work function (ϕ) values of 1T' MoS_2 with and without the H functional groups.

impede the formation of an ohmic contact. However, as shown by the experimental results, $r_{2H/1T'}$ is relatively small (~75 $\Omega \cdot \mu$m), thus demonstrating the ohmic nature of the 2H/1T' junction. To understand this apparent contradiction, the effects of surface adsorbates or functional groups in changing the charge density and thus the work

function of 1T' MoS_2 must be assessed. In fact, the adsorption of chemical species on the surface of 2D materials is known to modify their electronic properties. Given the chemical phase transition treatment that is applied in this work, which involves the formation of a lithium molybdenum sulfide (Li_xMoS_2) intermediate compound that requires a hydration reaction to remove the lithium content, the most probable adsorbates are hydrogen (H) functional groups[142]. Therefore, DFT calculations have been used to study the properties of H-doped 1T' MoS_2, where the H atoms are bonded to the sulfur atoms, which is the most favorable configuration. The results showed that H adsorption leads to further structural stabilization of the 1T' phase. The pristine 1T' phase is less stable than the 2H phase by 0.55 eV per MoS_2 molecule, but it becomes more stable by 0.16 eV per MoS_2 molecule with full H coverage of 0.5/Mo.

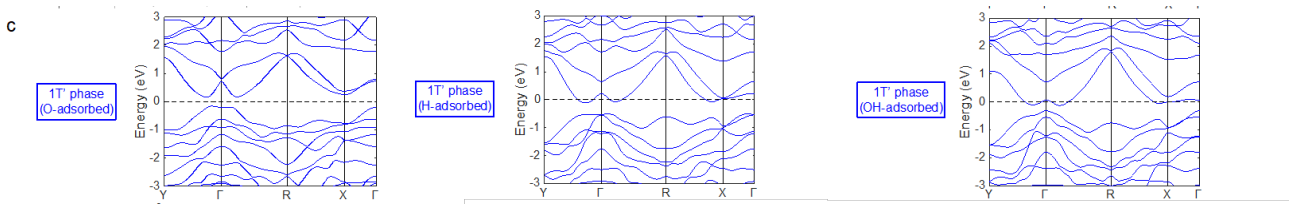


Figure 96. The band structures of the 1T' phase with the adsorption of functional groups at the coverage of 0.5/Mo.

An atomic model has then been constructed and we performed a structural relaxation analysis of the 2H/1T' MoS_2 junction with H adsorbed on the 1T' region only. The results showed that each phase remained stable after optimization and formed a stable boundary, which is in good agreement with the results of previous direct observations of 1T' and 2H phases in coexistence[145]. The relaxed atomic structure of their boundary are shown in Figure 97. We note that a recent theoretical work[173] reported the structural stability and electronic properties of a similar structure between the S-edge 2H MoS2 and 1T'

MoS_2. Here, we observed that H adsorption raises the Fermi level and therefore substantially reduces the work function of 1T' MoS_2 to about 4.4 eV at 0.5 H/Mo coverage, which eases ohmic contact formation by significantly reducing the energy barriers; this may also explain the small resistance observed in the 2H/1T' junction. More details about the effects of H adsorption as well as other functional groups, *e.g.* oxygen and hydroxyl (-OH) groups, on the stability and electronic structure of the 1T' phase are presented in the. The partial charge densities at the boundaries between 2H MoS_2 and H-functionalized 1T' MoS_2 as shown in Figure 97. The calculations show that the electronic states closest to the Fermi level are not only from the metallic 1T' phase, but also contain a substantial contribution from the atoms closest to the boundary in the semiconducting 2H phase. This lateral orbital overlapping, which stemmed from the seamless 2H/1T' interface, further guarantees the ease of electron transition across the 2H/1T' side-contact.

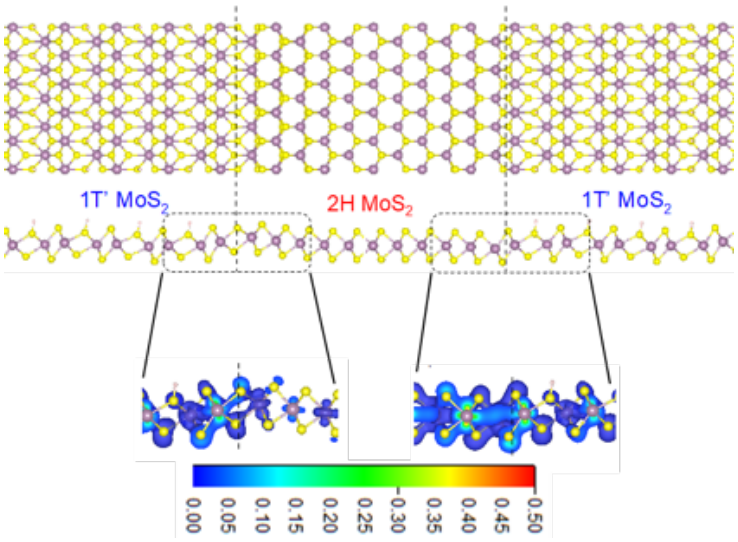


Figure 97. Calculated atomic structure of 2H/1T' MoS_2 boundary with H adsorbed on the 1T'-phase. Contour plots of partial charge densities associated with the states in the energy range of [E_F–1.0 eV, E_F] at the two boundaries between the 1T'- and 2H-phases are shown below. The numbers in the color bar are in units of $e/Å^3$. The isosurface levels are selected at 0.02 $e/Å^3$.

The partial charge density distribution on the side of the 1T' phase is very similar at the two boundaries; while on the 2H-phase side, the different edge (Mo-edge and S-edge) termination results in distinctly different density distributions.

Figure 98 shows contour plots of partial charge densities associated with the states in the energy range of [E_F–1.0 eV, E_F] at the two boundaries between the 1T'- and 2H-phases. The numbers in the color bar are in units of e/Å^3. The isosurface levels are selected at 0.02 e/Å^3. The partial charge density distribution on the side of the 1T' phase is very similar at the two boundaries.

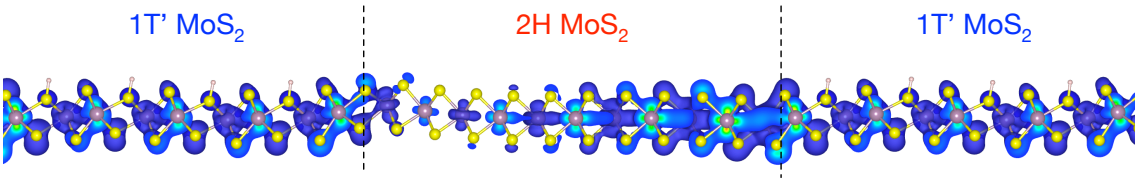


Figure 98. The partial charge density associated with the states in the energy range of [EF-1.0 eV, EF] for the entire device.

Finally, the performance of the fabricated device has been benchmarked against some state-of the-art sub-10 nm channel FETs in Table 4-2.

Table 4-2Benchmarking of sub-10 nm channel transistors

Channel	Si FinFET[174]	Silicon On Insulator[175]	Si SOI[176]	InGaAs[177]	CNT[178]	**MoS_2**
L_{ch} (nm)	10	9	8	6	9	**7.5**
EOT (Å)	17	40	12	25	6.5	**40**
SS (mV/dec)	125	300	90	750	94	**110**
I_{on}/I_{off}	10^5	10^4	9×10^2	4×10^2	10^4	**$>10^5$**

5 NOVEL APPLICATIONS OF FERROELECTRIC MATERIALS

This chapter will discuss the use of the ferroelectric HfO_2 material originally developed for HET applications in three novel applications. The first two use the "negative differential capacitance" properties of the ferroelectric materials, while the third application is based on analog modulation of polarization in a ferroelectric thin film.

5.1 Negative capacitance FET for sub-60 mV/decade SS

For decades, computer chips have been solely made of silicon. However, doubling the number of chips on the same integrated circuit area, and thus following Moore's law, is becoming increasingly challenging as silicon technology reaches its physical limit. Two main paths are currently being pursued to continue the scaling of CMOS technology in the next few decades: 1. finding a new channel material that would allow electronics to move beyond silicon in miniaturization of the transistor channel length, and 2. determination of a new device mechanism to overcome the thermionic limit in metal oxide semiconductor field effect transistors (MOSFETs), thereby enabling reduction of the power consumption by further reducing the supply voltage.

Recently, layered two-dimensional (2D) semiconducting crystals of transition metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), have been proposed to enable aggressive miniaturization of FETs [129-132]. The atomically-thin body thickness of TMDs improves the gate modulation efficiency. This can be seen in their characteristic scaling length[134], $\lambda = \sqrt{\frac{\varepsilon_{\text{semi}}}{\varepsilon_{\text{ox}}} t_{\text{ox}}. t_{\text{semi}}}$, where $\varepsilon_{semi}/t_{semi}$ and ε_{ox}/t_{ox} are the dielectric constant/thickness of the channel and oxide, respectively.

λ determines important short channel effects such as drain-induced barrier lowering and the subthreshold swing (SS). In particular, MoS_2 has a low dielectric constant of $\varepsilon = 4–7$[135, 136] and an atomically thin body ($t_{semi} \approx 0.7$ nm × number of layers), which facilitate the decrease of λ, while its relatively high bandgap energy (1.85 eV for a monolayer) and high effective mass allow for a high on/off current ratio (I_{on}/I_{off}) via reduction of direct source–drain tunneling[137]. These features make MoS_2, and wide-bandgap 2D semiconductors in general, interesting candidates for low-power subthreshold electronics. We have previously reported methods to reduce the channel length in MoS_2 FETs to 15 nm using graphene contacts (section 4.2)[131] and 7.5 nm using directed self-assembly patterning (section 4.3)[13]. Despite the advances made in TMD FET miniaturization, the power scaling in such devices suffers from the same issues than in Si MOSFET technology, where the supply voltage is limited by SS, which is the gate voltage change (ΔV_g) required to increase the source–drain current (I_{ds}) by one decade:

$$SS = \frac{dV_g}{d\psi_s} \times \frac{d\psi_s}{d(\log I_{ds})}$$

$$\frac{dV_g}{d\psi_s} = \left(1 + \frac{C_s}{C_{ins}}\right)$$

where C_s and C_{ins} are the semiconductor and dielectric insulator capacitance, k is the Boltzmann constant, T is the temperature, and q is the elementary charge.

Limited by thermionic emission, Boltzmann statistics limits the second term in the above formula to $\ln(10kT/q)$, which is about 60 mV/dec at room temperature. The first term, which is known as the body factor m, is always greater than one. Therefore, SS > 60 mV/dec at room temperature in a standard MOSFET, limiting the minimum supply voltage

possible for a given drain current capability. To lower the SS and, in that way, the supply power, we need to overcome the limit of at least one of the terms in the above formula.

To overcome the limit of $\frac{d\psi_s}{d(\log I_{ds})}$ a transport mechanism different from thermionic emission is required. The most widely studied method is tunnel-FETs, where carriers are injected into the channel by band-to-band tunneling from the source to the drain so over-barrier emission, as in MOSFETs, is circumvented. This theoretically allows steeper change of the current and thus overcomes the limit of 60 mV/dec. However, the experimental results reported so far severely suffer from the interface trap-assisted tunneling mechanism, which generates a large background current obscuring the steepness of turn on of the band-to-band tunneling[179] .

An alternative method to reduce the SS below 60 mV/dec in a MOSFET is to decrease the body factor to less than one[180]. This requires the capacitance to be mathematically negative (i.e., $C_{ins}<0$). The body factor is the inverse of the gate efficiency ($\beta = d\psi_s/dV_g$), which is the rate that the semiconductor surface potential ψ_s changes by changing V_g. Therefore, if $C_{ins}<0$ then $\beta>1$, a condition that is always impossible with conventional dielectric insulators.

A negative differential capacitance effect has been experimentally observed in ferroelectric materials during the phase transition when the system is in nonequilibrium[127]. In addition, sub-60 mV/dec switching characteristics have been observed in several negative-capacitance (NC) FETs using lead zirconate titanate[181], bismuth ferrite[182] and polymer ferroelectric dielectrics such as P(VDF)-TRFE[183, 184]. However, neither of these materials is technologically compatible with standard Si CMOS technology. In this regard, HfO_2 and ZrO_2[185] based ferroelectric materials are more favorable because they

are fully compatible with the CMOS manufacturing process and their thin films can be obtained by standard deposition techniques, such as atomic layer deposition (ALD), and they can thus be easily integrated into transistor structures. The HfO_2-based gate dielectric has been extensively developed for CMOS applications with well-defined ALD processing technology, and it is used in current technology nodes. In addition, robust ferroelectricity has been reported in thin-films of HfO_2 systems with various dopants, such as rare-earth[186], Si[187], and Al[188] dopants. By extending the ALD technology developed in chapter 1, Al-doped HfO_2 (Al: HfO_2) ferroelectric thin films has been used to develop NC-MoS_2 FETs. The incorporation of the NC mechanism in transistors with a 2D channel (e.g., MoS_2 FETs) could be a solution to extend the boundaries of transistor dimension scaling as well as power scaling, and extend Moore's law to its ultimate limit to enable the continued increase of the functionality of semiconductor electronics.

5.1.1 Ferroelectric HfO_2 thin film development by ALD

The atomic accuracy in the thickness of ALD films allows precise control of the molar ratio of the dopant to the host metal in bimetal oxide systems such as Al: HfO2. In our work, ALD Al:HfO_2 deposition was carried out at a substrate temperature of 250 °C using trimethylaluminum (TMA) as the Al precursor, tetrakis(ethylmethylamino)hafnium (TEMAH) as the Hf precursor, and H_2O as the oxidant. A Si wafer with a native SiO_2 layer was used as the substrate. The Al composition of the films was varied from 0% to 16.7% by controlling the TMA/TMHA pulses. The ALD process consisted of TMA cycles in the middle of sequences of TEMAH cycles. After deposition, the samples were rapid thermal annealed (RTA) in forming gas at 850 °C for 5 min to crystallize the films and intermix Al with the HfO_2 body to form a homogenous Al: HfO2 matrix.

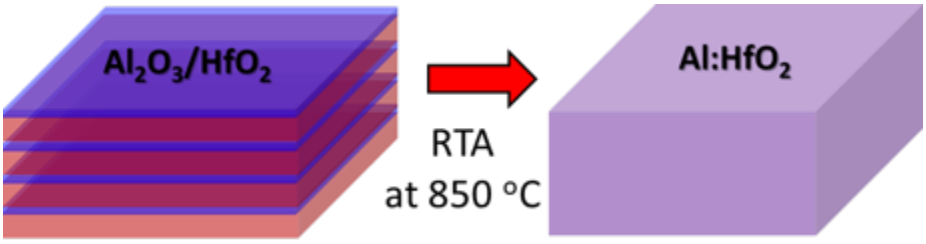


Figure 99 Schematic representation of ALD supercycle used for doped HfO_2 development

XPS analysis was performed on the Al: HfO2 films after varying the ratio of TMA cycles to TEMAH cycles (Figure 100 (a) and (b)). Figure 100(c) shows a plot of the Al content of ~10 nm thin films extracted from the XPS analysis versus the TMA/TEMAH cycle ratio. The linear fit with near unity slope shows that the Al content can be precisely controlled in the range 0%–16.7%. Moreover, in-depth analysis showed negligible variation in the Al content after different etching times by Ar plasma, which indicates that the Al dopant atoms are uniformly dispersed in the HfO_2 lattice. This process can be repeated for many other dopants (i.e. Zr, Si, Gd, Y, Sc etc.) where the dopant concentration and annealing conditions depends on the phase diagram of the particular system.

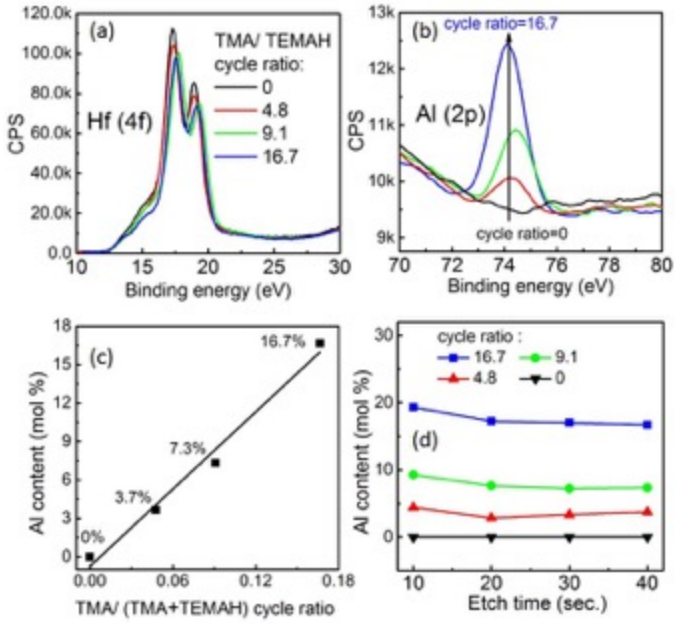


Figure 100(a) and (b) XPS analysis of Al-doped HfO_2 films with different Al contents deposited on Si wafers with TMA/TEMAH cycle ratios ranging from 0 to 16.7%. (c) Al content of the Al: HfO_2 films extracted from the XPS spectra shown in (a) and (b) as a function of the TMA/TEMAH cycle ratio. The inset shows as a schematic of the deposited stacked HfO_2 and Al_2O_3 and homogeneously Al-doped HfO2 (Al: HfO_2) formed after RTA. (d) Al contents for different etch times.

Figure 100(a) compares the grazing incident X-ray diffraction (GIXRD) patterns of the undoped and 7.3% Al:HfO_2 samples. The XRD analysis suggests a phase transition from the monoclinic phase to the orthorhombic phase upon doping. This noncentrosymmetric transition phase is a prerequisite for ferroelectric characteristics. Next, we analyzed the ferroelectric capacitor with a 10 nm 7.3% Al: HfO2 film. For this measurement, a highly doped Si wafer was used as the back electrode and Ni pads were patterned on the thin film as the top electrode. An extra RTA step was performed at 450 °C after deposition of the Ni electrodes to eliminate charged interfacial trapped states.

Figure 101 (b) shows plots of the polarization versus electric field (*P–E*) hysteresis loop of 10 nm 0% and 7.3% Al: HfO2 capacitors. Compared with the undoped sample, the 7.3%

sample shows a P–E hysteresis loop, which confirms the ferroelectricity of the ALD grown thin film with a coercive field of 1.55 MV/cm and remnant polarization of 9.5 μC/cm^2. Figure 101(c)–(e) show the transient voltage (V_F), current (I_R), and charge (Q) of the capacitor on application of a square voltage pulse (Vs). A schematic of the measurement setup is shown in the insert of Fig. 2(d). I_R is determined by $I_R = (V_s - V_F)/R$, where R is a 10 KΩ resistor and Q is calculated using $Q = \int I_R(t)dt$. The regions of interest are marked with dashed lines in Figure 101(c) and (e), where V_F and Q show different trends and dV_F/dt and dQ/dt have opposite signs. This indicates the presence of a negative capacitance feature in these regions ($C = dQ/dV < 0$).

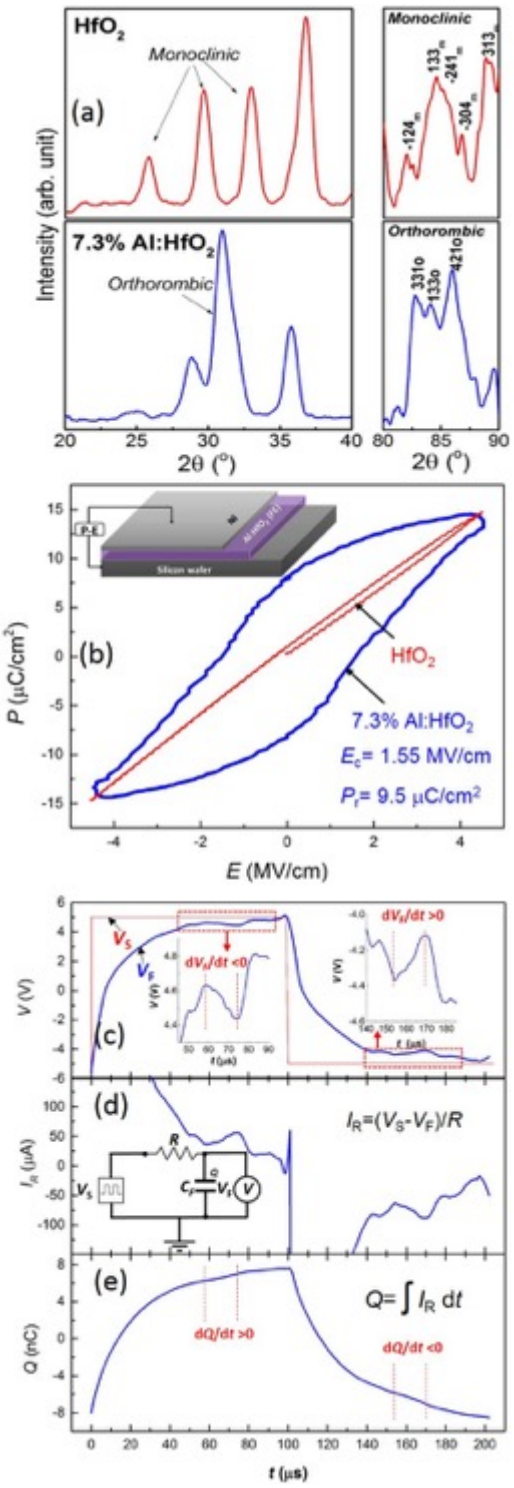


Figure 101. (a) GIXRD patterns of undoped and 7.3% Al-doped HfO_2. (b) Polarization versus electric field hysteresis of undoped and 7.3% Al-doped HfO_2. (c-e) Transient voltage, current, and charge of 10 nm 7.3% Al-doped HfO_2 with a 200 μs period. The insert of (d) shows a schematic of the measurement setup.

5.1.2 Transport characteristics of negative capacitance MoS_2 FETs

As previously discussed, the aim of incorporating a ferroelectric material in the gate stack of a MOSFET is to increase the gate efficiency above one by exploiting the NC effect of the ferroelectric material. Regardless of its absolute value, any NC can make the gate efficiency greater than one. However, it should be noted that the total gate capacitance C_g has to remain positive to avoid instability in the system, which requires that $|C_f|>C_s$ (where C_f is the ferroelectric NC), otherwise it will result in strong hysteresis during device operation[189]. This condition can fail because C_s is a nonlinear function of V_g and V_d, which can push the transistor to an instable condition during its transition from depletion (low C_s) to the inversion condition (high C_s). To guarantee stabilization in the whole operation regime, a positive-capacitance dielectric oxide (C_{ox}) can be added in series with the ferroelectric dielectric layer and the semiconductor. In this bilayer configuration, $|C_f|$ has to be greater than the oxide dielectric capacitance ($|C_f|>C_{ox}$) to amplify the gate efficiency ($\square>1$) and greater than $C_{mos}=(C_s+C_{ox})^{-1}$ to meet the stability condition ($C_g>0$), which is always the case as long as the first condition ($|C_f|>C_{ox}$) is met.

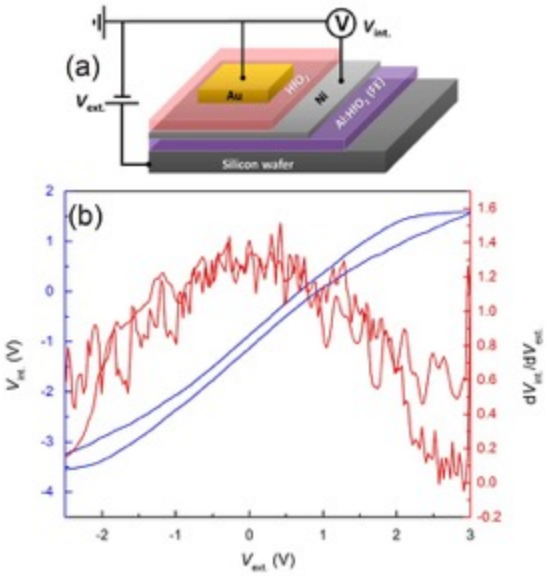


Figure 102. (a) Schematic of the measurement setup used to characterize the potential amplification in the nominal 10-nm-Al: HfO_2/10-nm-HfO_2 bilayer system with a Ni intermediate electrode. V_{ext} was applied to the Si wafer and the induced potential on the intermediate Ni electrode V_{int} was read in voltage mode (voltmeter). (b) V_{int} and dV_{int}/dV_{ext} versus V_{ext}.

We used undoped HfO_2 as the positive-capacitance oxide component in the bilayer gate stack. To protect the surface potential in the device against the charge nonuniformity induced by microdomains in the ferroelectric film, the ferroelectric and the normal dielectric layers need to be separated by a metal layer to average out such non-uniformities[190]. To evaluate the potential amplification in the bilayer structure, we fabricated a test capacitor structure composed of Ni pads formed on the 10 nm 7.3% Al:HfO_2/Si substrate, a 10 nm HfO_2 layer deposited on the Ni pads by ALD, and Au top electrodes deposited on the HfO_2 layer (see Figure 102(a)). In the device, contact holes were etched through HfO_2 to access the intermediate Ni layer.

Figure 102 (b) shows a plot of the potential of the intermediate Ni electrode V_{int} versus the potential applied to the doped-Si substrate, V_{ext}, when the top electrode is grounded. This shows how much V_{int} can be amplified by the NC effect. Using the capacitor divider method, the amplification factor is $dV_{int}/dV_{ext} = [1/ (1+C_{ox}/C_f)]$. The factor monotonically increases, exceeds one at $V_{ext} \sim -1.5$ V, and reaches an average maximum gain of ~1.25. This confirms that the bilayer NC stack works properly and can potentially enhance the switching rate of a transistor when used as the gate stack.

Next, we fabricated MoS_2 FETs by transferring an exfoliated tri-layer MoS_2 film onto the bilayer gate stack and formed source/drain contacts by electron-beam lithography. Figure 103(a) and (b) show schematics of the NC-MoS_2 FET with a bilayer gate stack and the reference MoS_2 FET with only HfO_2 as the gate dielectric. Figure 103(c) compares the transfer characteristics of the reference and NC devices. The measurements were performed in vacuum to eliminate the hysteresis induced by physioabsorbed moisture on the MoS_2 channel. Both devices show small hysteresis (17mV). In the case of the NC FET, this confirms that the NC is stabilized in the entire swept range by using the bilayer configuration. The device has an on current of 5 μA/μm and maximum transconductance of 12 μS/μm, and the off current is as low as 1 pA/μm. The subthreshold characteristics of the device are of particular importance. In Figure 102(b), the developed gate stack allows internal gain of up to 1.25 times. This internal gain can improve the subthreshold swing of the transistor and allows the 60 mV/dec limit to be overcome without changing the transport mechanism. As shown in Figure 103(d), the reference device has SS_{min} = 67 mV/dec at a current level of ~10 pA/μm ((d)). The deviation of the SS from 60 mV/dec is attributed to trapped charges at the MoS_2/oxide interface, which lower the gate efficiency

and thus increase the SS. The NC FET with the same MoS_2 channel length and thickness as well as the same MoS_2/oxide interface shows significantly improved SS with a minimum of 57 mV/dec, which is in agreement with the observed voltage amplification in Figure 102(b). For the NC-MoS_2 FET, this allows transistor operation with $I_{off} \approx 10$ pA/μm and $I_{on}/I_{off} > 10^5$ with a ΔV_{gs} of 0.5 V compared with a required ΔV_{gs} of ~0.65 V to achieve the same performance in the reference MoS_2 FET. Because the channel/oxide interface can degrade the SS, the SS can be further reduced by developing an ultraclean MoS_2/oxide interface. Moreover, further optimization of the capacitance matching in the bilayer stack can improve the voltage amplification factor and thus further increase the gate efficiency. It should be noted that NC technology is in its infancy and several aspects need to be experimentally investigated. In particular, for targeted applications in state-of-the-art high-performance CMOS technology, the switching performance of NC FETs and the effects of dielectric thickness scaling and the gate-leakage current at high gate switching speeds on the amplification capability of the NC bilayer stack need to be extensively investigated.

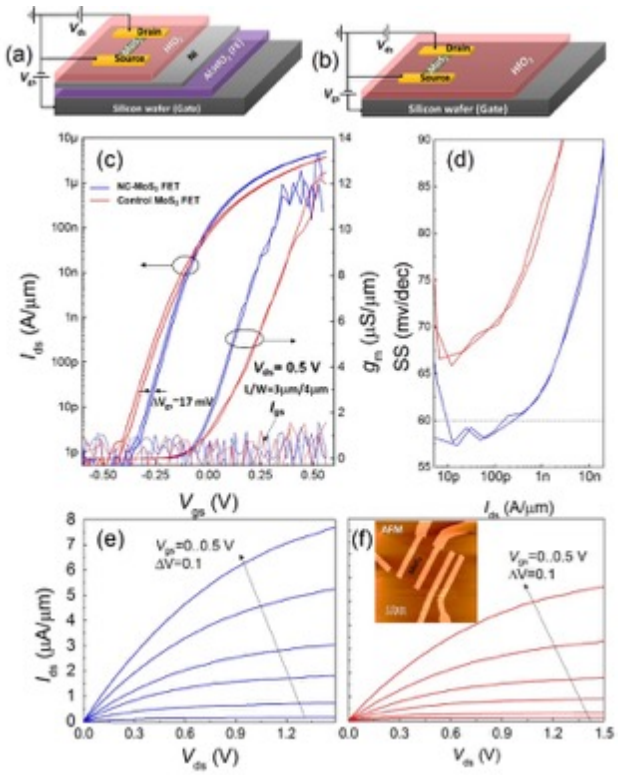


Figure 103. *(a)* Schematic of the NC-MoS_2 FET with an HfO_2/Al:HfO_2 bilayer stack with Ni used as the intermediate metal. (b) Schematic of a reference regular MoS_2 FET with a HfO_2 gate dielectric. In both (a) and (b), a highly doped Si wafer is used as the back gate. (c) Transfer characteristics and transconductance of the NC-MoS_2 FET and reference MoS_2 FET at room temperature. (d) Comparison of the SS of the NC-MoS_2 FET with that of the reference MoS_2 FET. (e), (f) Output characteristics of NC-MoS_2 FET and control MoS_2 FET, respectively. The inset in (f) shows an AFM image of a MoS_2 FET.

5.1.3 Effect of different dopants (Si, Zr) on the ferroelectric HfO_2

Although the Al doped HfO_2 shows ferroelectric characteristics, the thermal budget of the process is relatively high which may not be suitable for front end integration for most of the system. To circumvent this problem, other dopants like Si and Zr can be used.

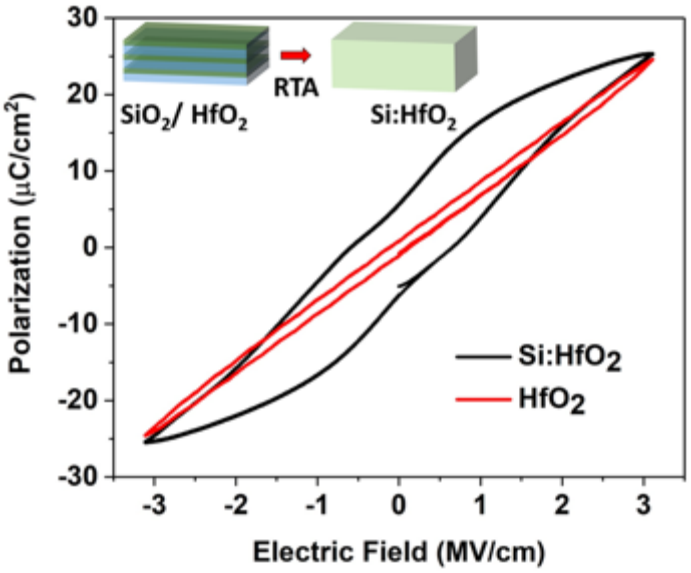


Figure 104 Polarization loop of 3.8% Si doped HfO_2 compared against HfO_2.

Figure 104 shows the polarization characteristics of TiN/15 nm 3.8% Si doped HfO_2/ TiN capacitor annealed at 650°C which can be lowered down 500°C in case Zr doped HfO_2.

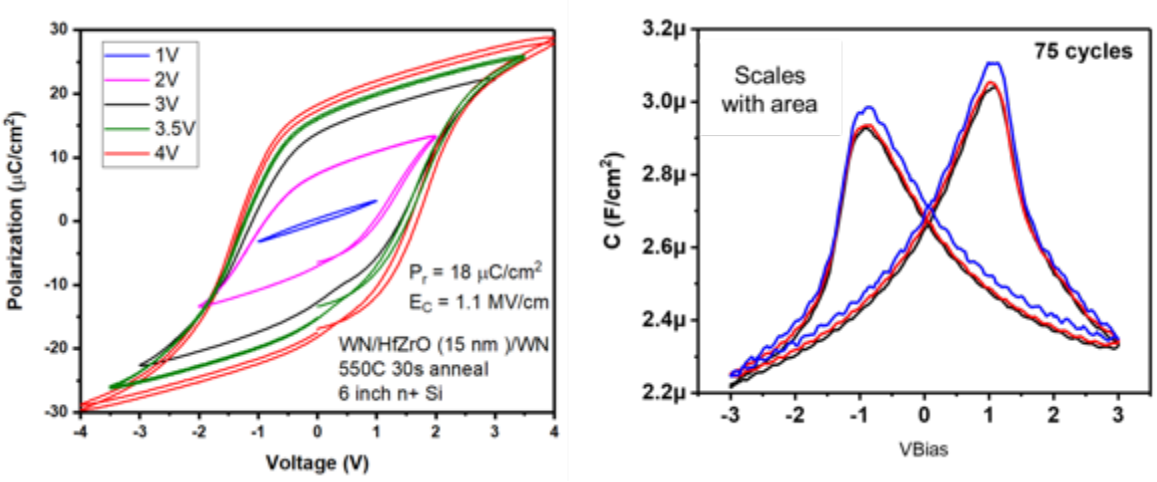


Figure 105 (a) polarization and (b) butterfly like C-V characteristics of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric annealed at 550°C.

5.2 MIT Virtual Source negative Capacitance Model (MVSNC)

In section 4.4.1, the MVS model has been used to study the transport in highly scaled MoS_2 transistors. Here, the same model will be extended by adding the physics of ferroelectric to study novel applications. This work presents a new, comprehensive, physics-based compact Verilog-A model, the MIT Virtual Source Negative Capacitance FET (MVSNC) model that describes transistors with ferroelectric (FE)-oxides in their gate-stack. The model combines the concept of virtual-source carrier-charge-injection for the computation of channel-current and charges in the underlying baseline transistor, together with the Landau-Khalatnikov (L-K) equation and the Preisach model to capture the polarization switching characteristics of the FE-oxide. The model provides a framework to evaluate novel device ideas and their impact at the system-level, which is particularly timely due to the recent surge in interest in the application of doped HfO_2 ferroelectric-transistors for logic, radio-frequency (RF) and neuromorphic applications [191-195]. The model, calibrated against device-measurements, is used for two example case studies: (i) to evaluate the design principles and performance capabilities of Negative Capacitance FETs (NCFETs) optimized for high frequency (RF and mm-wave) applications, and (ii) to test the scalability of FeFET analog synapses. The results provide improved device-design, and assess the impact of device-performance on the system-level learning-performance in a multilayer perceptron neural network simulation[196].

5.2.1 MVSNC model: Modeling methodology

The core MVS model uses the same set of equations mentioned in section 4.4.1. In addition, the fringing capacitances such as overlap ($Q_{S,ov}$, $Q_{D,ov}$), inner-fringing ($Q_{S,if}$, $Q_{D,if}$) charges, and body charges (Q_B) are included in the MVSNC model as described in [197] and contribute to the FE-oxide charge (Q_{GFE}) that

determines its dynamic behavior. The field-lines of the outer-fringing charges ($Q_{S,of}$, $Q_{D,of}$), on the other hand, do not permeate the FE-oxide and do not contribute to its transient dynamics, and are linked to external gate-terminal (V_G) as shown in Figure 106 (a).

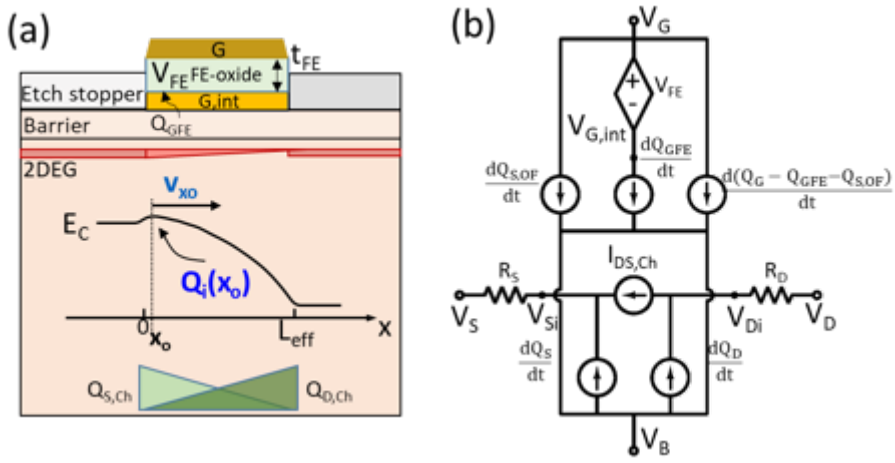


Figure 106 Typical cross-section schematic of (a) RF-NC-HEMTs and FeFETs, (b) equivalent sub-circuit diagram of MVSNC model with L-K equation

Current NCFET devices have two gate-stack options that differ by the presence (Type I) or absence (Type II) of an internal-gate-metal layer (Gint in Figure 106(a)). The MVSNC model can account for both types with appropriate computation of Q_{GFE} (and in-turn compute V_{FE}) as follows:

$$Q_{GFE} = -(Q_{S,Ch} + Q_{D,Ch} + Q_{S,if} + Q_{D,if} + Q_{S,ov} + Q_{D,ov} + Q_B)$$

$$Q_{GFE} = -(Q_{S,Ch} + Q_{S,if} + Q_{S,ov} + Q_B)$$

(3)

The first expression above accounts for the charges from the underlying FET that are reflected in the internal-gate in Type I devices, while only the charges reflected at the VS-point as in the second expression are used in Type II devices. In both case we assume that there are no leakage paths through the dielectric [8]. The physical nature of the MVSNC model and its convergence robustness in system-level simulations is demonstrated using two example case-studies: (i) InGaAs-based RF-NCFET for high-frequency applications, and (ii) Si-CMOS based FeFETs for analog synaptic simulations. The dynamic L-

K equation given below:

$$V_{FE} = \alpha Q_{FGFE} + \beta Q_{FGFE}^3 + \rho \frac{dQ_{GFE}}{dt} \quad ;$$

$$\alpha = -\frac{3\sqrt{3}E_C}{4P_0} \quad ; \; \beta = \frac{3\sqrt{3}E_C}{8P_0^3}$$

with E_c=800 kV/cm^2 and p_0=8 μC/cm^2 is used to represent commonly used FE oxide Zr-HfO_2 [197]. It must be noted here that although the model accounts for viscous-damping term ϱ this is chosen to be arbitrarily small to make the intrinsic-polarization switching time-constant (τ_{PE}) in the ps-range so that it does not play a role in the RF-NCFET performance study. It has been noted elsewhere that device-scaling reduces τ_{PE} [198], but more work is necessary to assess the validity of this hypothesis.

Table 5-1 MVSNC model parameters for RF- and neuromorphic study

Model parameter	RF-NC HEMT	FEFET synapse
L_g :Gate-length	40 nm	40 nm
W_g :Gate-width	100 mm	100 nm
C_g:Areal gate capacitance	1.56 x10^{-6} F/cm^2	2.55 x10^{-6} F/cm^2
R_s,R_d:Contact resistance	140 Ω-mm	71 Ω-mm
m_0:Carrier mobility	2200 cm^2/Vs	135 cm^2/Vs
v_{x0}:Carrier velocity	5 x 10^7 cm/s	1 x 10^7 cm/s
C_{of}: Outer-fringing capacitance	2.25 x10^{-12} F/cm	1.84 x10^{-12} F/cm
C_{if}:Inner-fringing capacitance	-	1.5 x10^{-12} F/cm
E_c:Coercive field	800 kV/cm^2	800 kV/cm^2
P_0:Polarization charge	8 mC/cm^2	8 mC/cm^2
t_c:VDST time-constant	10 ns	10 ns

5.2.2 Case study: RF-NCFETs to enable near-THz operation

The MVSNC model is first calibrated against state-of-art baseline (t_{FE}=0 nm) E-mode L_g=40 nm $In_{0.7}Ga_{0.3}As$ metamorphic-HEMTs (MHEMTs) on GaAs substrate with record f_T=688 GHz and f_{max}=800 GHz [199].

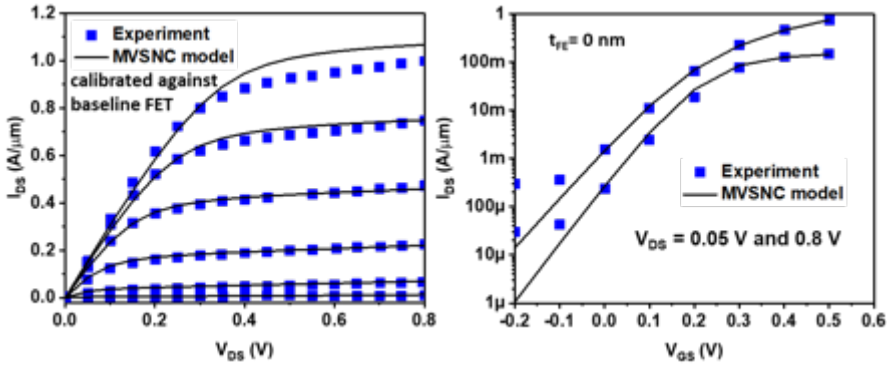


Figure 107 The MVS-model is calibrated against measured terminal-transport characteristics such as (b) output and (c) transfer curves of the baseline E-mode L_g=40 nm $In_{0.7}Ga_{0.3}As$ metamorphic-HEMT (MHEMT)[199].

As shown in Figure 107, the device-terminal output and transfer currents along with their derivatives are captured well. The key parameters are based on physical grounding; such as μ_0=2200 cm^2/Vs, v_{x0}=5x10^7 cm/s, R_s=R_d=140 Ω.mm and C_g=1.5x10^{-6} F/cm and are either extracted from independent device-measurements or are values normally reported for InGaAs-based HEMTs. Further, the device-level parasitics such as pad- and fringing-capacitances, lead-inductance, gate-resistance (R_g) are extracted from measured S-parameters. The resulting model is able to capture the small signal performance metrics accurately such as current gain (h_{21}), maximum-stable-gain (MSG), stability factor (k) along with the correct estimation of the f_T/f_{max} as shown in Figure 108 .

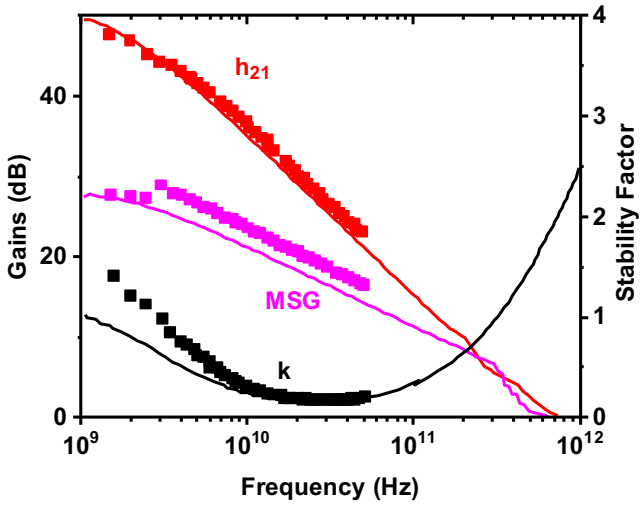


Figure 108 The device-charges and parasitics are captured to enable the accurate estimation of small-signal metrics such as current gain (h_{21}), maximum stable gain (MSG) and stability factor (k) as shown in (f). The baseline device exhibits $g_{m,max}$ = 2.7 mS/μm, f_T = 688 GHz and f_{max} = 800 GHz.

The calibrated model is then used to evaluate the RF-NCFET performance by activating the L-K equation for various t_{FE} from 5 to 25 nm. Both device types (I and II) are considered. The device-terminal currents for different t_{FE} indicate that, for the same voltage swing, the on-current (I_{on}) is higher by ~2x for the same off-current (I_{off}) due to internal-gate amplification, albeit to a lesser extent in Type II devices. Further, both scenarios at larger t_{FE} show hysteretic and negative-g_{DS} profiles as can be seen from the output curves in Figure 109.

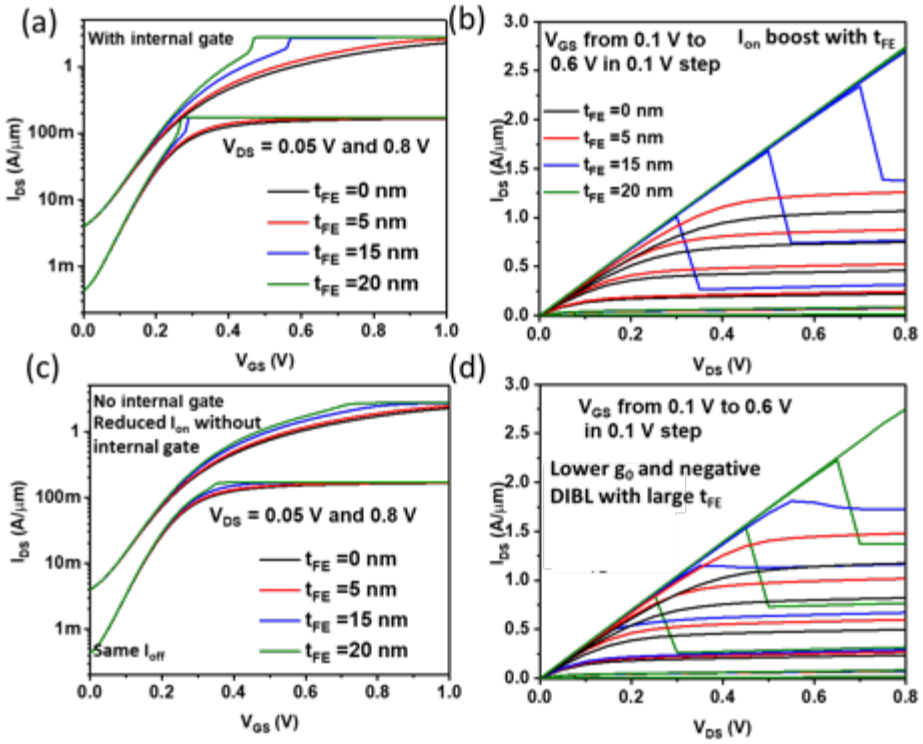


Figure 109 (a-b) show the terminal-output and transfer characteristics of Type-I device as a function of FE-oxide thickness (t_{FE}) with internal-gate showing enhanced on-current (I_{on}) (up to 2x) for the same off-current (I_{off}) as well as reduced SCE such as DIBL and n_d. (c-d) The terminal characteristics of Type-II device also show similar behavior as in (a-b) albeit with reduced extent of I_{on}-amplification (1.4x) and SCE-reduction since Q_{GFE} is lower in this device.

This is due to reduced V_{Gint}-amplification ($dV_G/dV_{Gint}=|C_{FE}|/C_{DE}-|C_{FE}|$) with V_{DS} as channel-capacitance decreases with V_{DS}. This expected reduced DIBL, compensates the one due to the Short Channel Effect (SCE) of such scaled RF-devices, and improves overall intrinsic-gain and RF-metrics of the device as discussed below.

The small-signal simulations for both device types are shown in Figure 110 and Figure 111 and indicate boost in h_{21} (by 8 dB and 4 dB in Types I and II respectively), while the associated f_T is boosted as well (by as much as 150 GHz). The reduced-DIBL effect is manifested in S_{22} plots in both device-types which improves the intrinsic-gain (g_m/g_{DS}) by ~4x in Type I and by 30% in Type II. Enhancement of S_{21} in Figure 110(d)-Figure 111(d) by 18 dB in Type I and 5 dB in Type II translates to f_{max} enhancement as shown in Figure 110(f)-Figure 111(f).

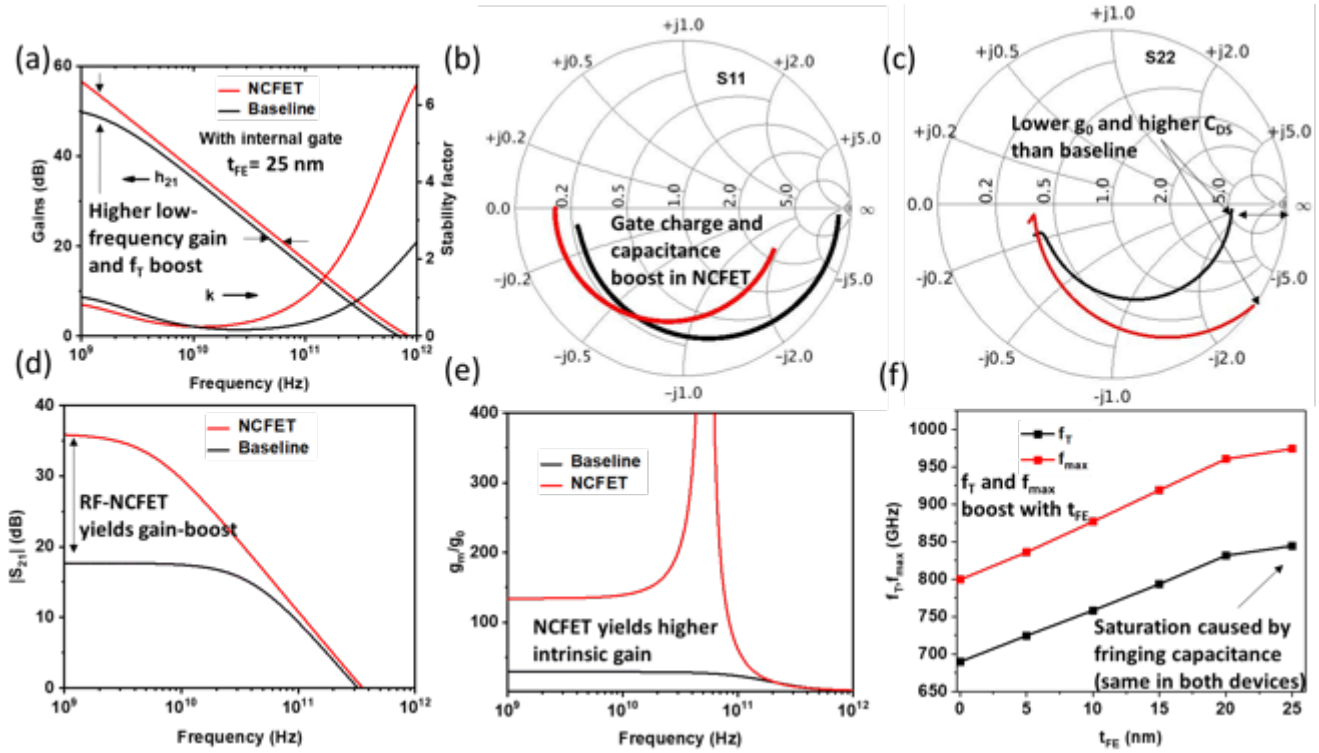


Figure 110 RF-performance of Type-I device (with t_{FE}=25 nm) compared against baseline for V_{DS}=0.6 V and I_{DS}=0.3 mA/μm: (a) the low-frequency h_{21} is enhanced by 8 dB along with f_T-boost by 20%. (b) The $V_{G,int}$-amplification and gate-charge (Q_G)-enhancement manifests in S_{11}. (c) The reduced g_{DS} in Type-I device compared baseline is evident as S22 is starting from close-to infinite-impedance point at lowest frequency on the smith-chart. Enhancement of S_{21} by 18 dB in (d) and intrinsic-gain (g_m/g_{DS}) by ~4x is shown. (f) The device-f_T and f_{max} can be significantly boosted (by ~150 GHz each) through careful selectin of t_{FE} with diminishing returns at higher t_{FE} due to the parasitic-fringing device-capacitances along with instability issues. This study shows the potential of gate-stack engineering for high-performance RF-device fabrication.

The diminishing returns in f_T/f_{max}–boost with t_{FE} is because of the capacitive-loadline offered by the constant extrinsic-outer fringing capacitances ($C_{S,of}$, $C_{D,of}$) which limit the performance gains at high t_{FE}-regimes. This study illustrates the advantages of integrating FE-oxide with scaled high-performance RF-HEMTs (provided τ_{FE}~0 can be proven experimentally) to further boost the operating frequency ranges into the near-THz regimes. The MVSNC model can also provide a framework for device-designers for selecting gate-stack (FE-oxide) dimensions and composition to fabricate RF-NCFETs for targeted applications.

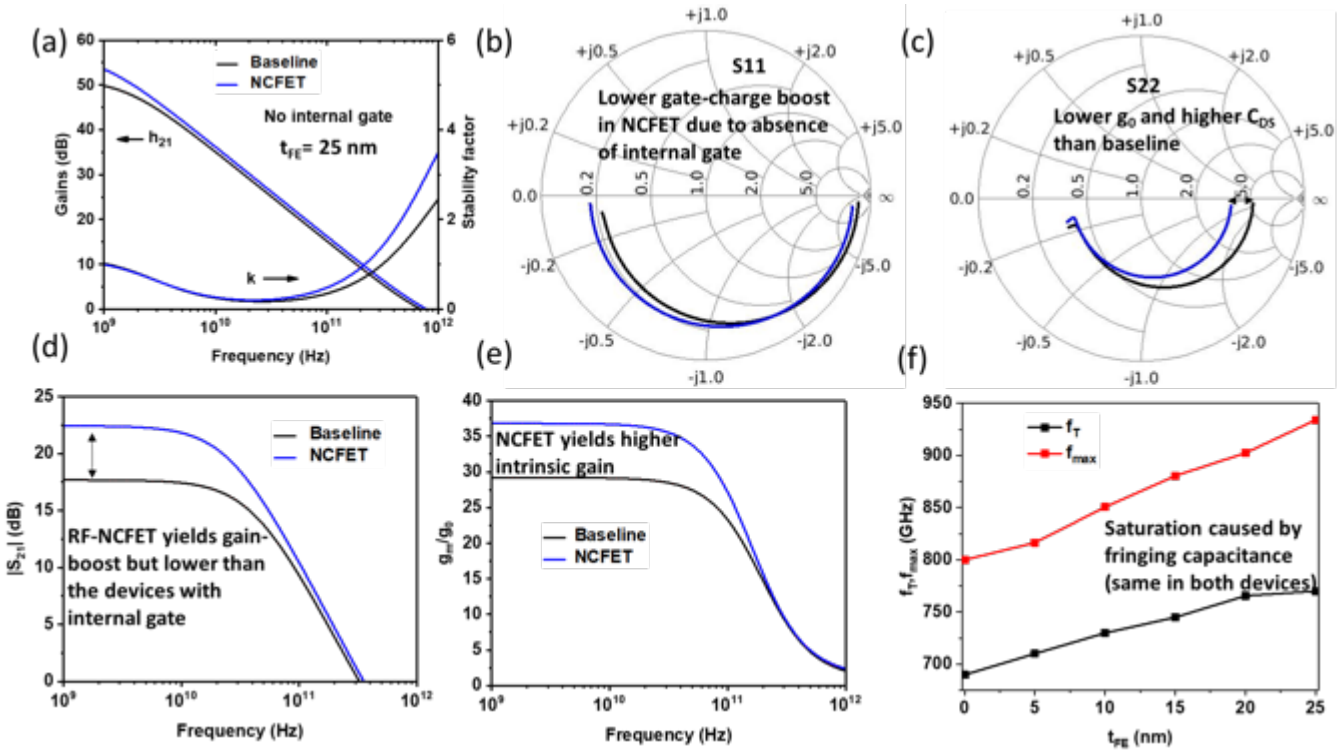


Figure 111 RF-performance of Type-II device compared against baseline for the same t_{FE} and bias-point as in Fig. 4: (a) low-frequency h_{21} enhancement is lowered than in Type-I case (~4 dB) along with f_T-boost by 8%. (b) The $V_{G,int}$-amplification and gate-charge (Q_G)-enhancement is also reduced due to lower contribution of channel-charge to Q_{GFE}. (c) g_{DS} is still reduced in Type-II device compared baseline while S21 is enhanced by 5 dB in (d) and intrinsic-gain (g_m/g_{DS}) by 30% as shown in (e). (f) The device-f_T and f_{max} also show improvement (~150 GHz each, subdued compared to Type-I).

5.2.3 Experimental Demonstration

To validate the simulation presented in the previous section, GaN/InAlN HEMT structure presented in is being used. However, the ferroelectric integration is being done at the backend rather than at the gate stack. The idea is to demonstrate type I devices with internal gate. After the baseline GaN HEMTs

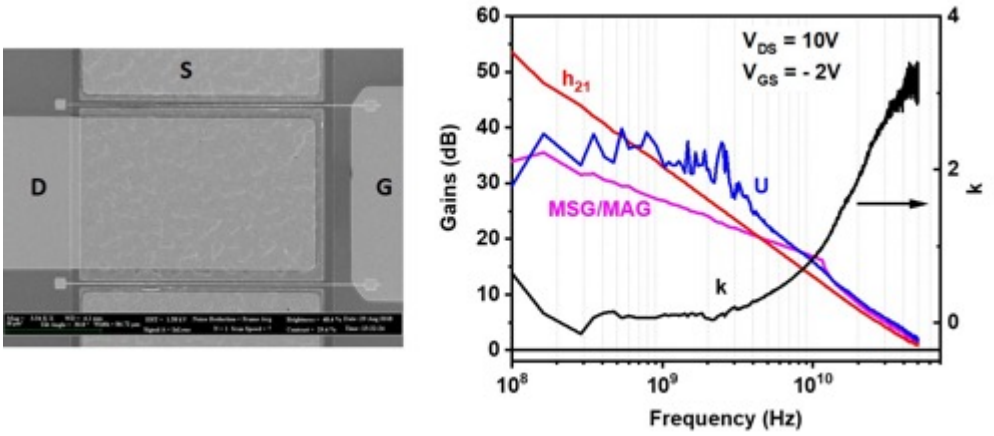


Figure 112 (a) SEM image and(b) measured high frequency gains of a baseline InAlN/GaN HEMT with L_g= 150 nm .

fabrication, the FE capacitor will be built on the gate pad to provide coupling to the device. In this way, the FE cap technology can be integrated into any pre-fabricated transistors.

5.3 MIT Virtual Source Ferroelectric Model (MVSFE)

The MVSNC model describes the FE-oxide-behavior using both the dynamic L-K equation. To capture the physics of the memory devices we include dynamic Voltage Dependent Switching Transient (VDST) and static Preisach models in MVS ferroelectric (MVSFE) model. While the appropriate physics is still under study, the Verilog-A integrates both models using a flag to select between MVSNC and MVSFE. The second set of equations in MVSFE model for the FE-oxide combines dynamic VDST model [200] and static Preisach model[201] to model V_{FE} as shown in Figure 113(d) to capture the statistical nature of multi-domain partial polarization switching, minor-loop and memory wipe-out effects:

$$F_{\pm} = Q_{sat}\, tanh\left[\frac{\left(V_{G,int\tau} - V_{C\pm}\right)}{V_{scaling}}\right]$$

$$; \frac{dQ_{GFE}}{dt} = \frac{Q_{sat}}{V_{C\pm}}\frac{dV_{FE}}{dt}\left[\frac{Q_{GFE}-Q_{GFE,last}}{F_{\pm}-F_{\pm,last}}\right]\left[1+\left(\frac{F_{\pm}}{Q_{sat}}\right)^2\right]$$

$$\tau_i = \tau_{\infty}\, exp\left(\frac{V_{0i}}{V_G - C_i - \frac{\left(V_{G,int\tau}-C_i\right)^x}{\left(V_G-C_i\right)^{x-1}}}\right)^m$$

Four domains (i=1-4) are considered with τ_{∞}=10 ns, m=1, x=1-2 and $Q_{sat}=P_0WL_g$, $V_C=E_Ct_{FE}$ have usual

meanings described in [200, 201]. In MVSFE model, the sign of $\frac{dV_{FE}}{dt}$ determines the hysteretic-branch of Q_{GFE}-V_{FE}, while V_{FE} in comparison to V_c determines whether the FE-oxide operates in major or minor loop under transient conditions.

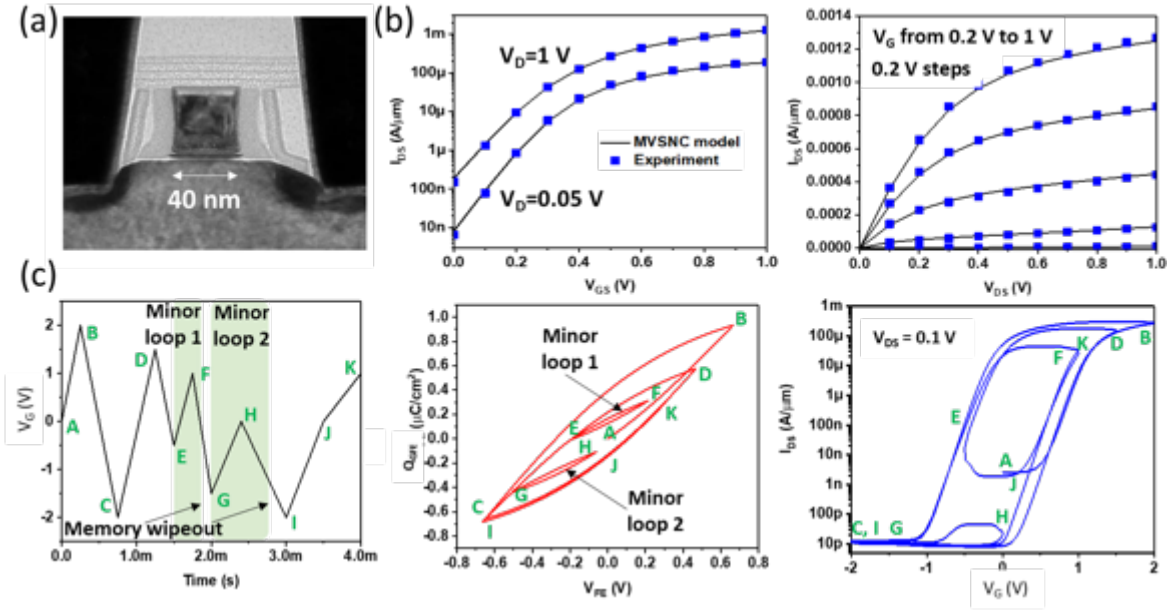


Figure 113 (a) SEM image of Intel-45 nm N-FET which is used as the baseline device technology for the FeFET analog synapse simulation-study [13]. (b) The MVS-model is calibrated against measured "standard" device-output and transfer characteristics along with the inclusion of device-level parasitic capacitances (c) The simulated response of the 45 nm-neuromorphic FET to an arbitrary V_G-pulse is shown in terms of Q_{GFE}-V_{FE} characteristic of FE-oxide as well as device-transfer characteristic. The minor-loop creation when dV_{FE}/dt changes sign along with memory-wipeout when V_{FE} crosses the corresponding V_c of minor loop are simulated using the MVSFE model and the corresponding shift (and hysteretic behavior) in transfer-curves can be seen.

5.3.1 Analysis and design of scaled-L_g FeFET synapses using MVSFE model

The MVSFE model is also used to evaluate the impact of technology scaling on the system-level performance of FeFET synapses based on polarization switching. FeFET analog synapses are 3-terminal devices that have been proposed to improve the classification accuracy and yield low latency in non-volatile memory-based neuromorphic accelerators. This is due to their high conductance ratio, sub-100 ns pulse based operation [191]and seamless integration with CMOS process flow. A weight update pulse is applied to the gate of the device to create multi-valued conductance between source and drain. The

MVSFE framework is used to evaluate the weight update characteristics and key parameter matrices (G_{max}/G_{min}, linearity, symmetry) which determine the classification accuracy in Deep Neural Network (DNN) [202]of such scaled synapses for different potentiation/depression schemes with 5-bit input voltage schemes (of arbitrary pulse-widths, amplitudes and read-times).

Intel-45 nm node [203] is selected as the baseline technology node which is highly scaled compared to earlier work in [191]. The baseline model is first calibrated against the measured device characteristics as shown in Figure 113 (b). The standard dielectric in the FET is replaced with FE-oxide to access the impact of baseline-MOSFET technology scaling on the performance capability of pseudo-crossbar arrays of analog synapses based on partial polarization switching characteristics of FeFETs. The dynamic VDST and static Preisach models are activated for FE-oxide (t_{FE}=10 nm) and for an arbitrary V_G-input, it can capture both minor-loop formation and memory-wipeout as shown from Q_{GFE}-V_{FE} and I_{DS}-V_{GS} curves of Figure 113(c).

Three different potentiation/depression pulsing schemes are applied to the device and the simulated Q_{GFE}-V_{FE}, I_{DS}-V_{GS} and conductance (S) profile vs. pulse count (32 counts, 5-bits) are shown in Figure 114. The constant pulsing scheme (I) does not let the FE-oxide traverse multiple minor Q_{GFE}-V_{FE} loops and shows constant S-profile. The other two schemes (variable pulse-width (II) and variable pulse-height (III)) show promise for FeFET as an analog synapse since they show G_{max}/G_{min} ratios of 47, 122 respectively. The shape of the profile is closer to linear-response indicating the deterministic partial switching of FE-domains. The variable-height scheme offers the greatest linearity as in [191]and offers similar G_{max} values at reduced device-width and hence footprint, an advantage accrued from technology-scaling. Time-period (T_P=2 ns and programming ($T_{PW,pot(dep)}$=65 ns) are reduced compared to [3] due to the L_g-scaling, thus improving the latency.

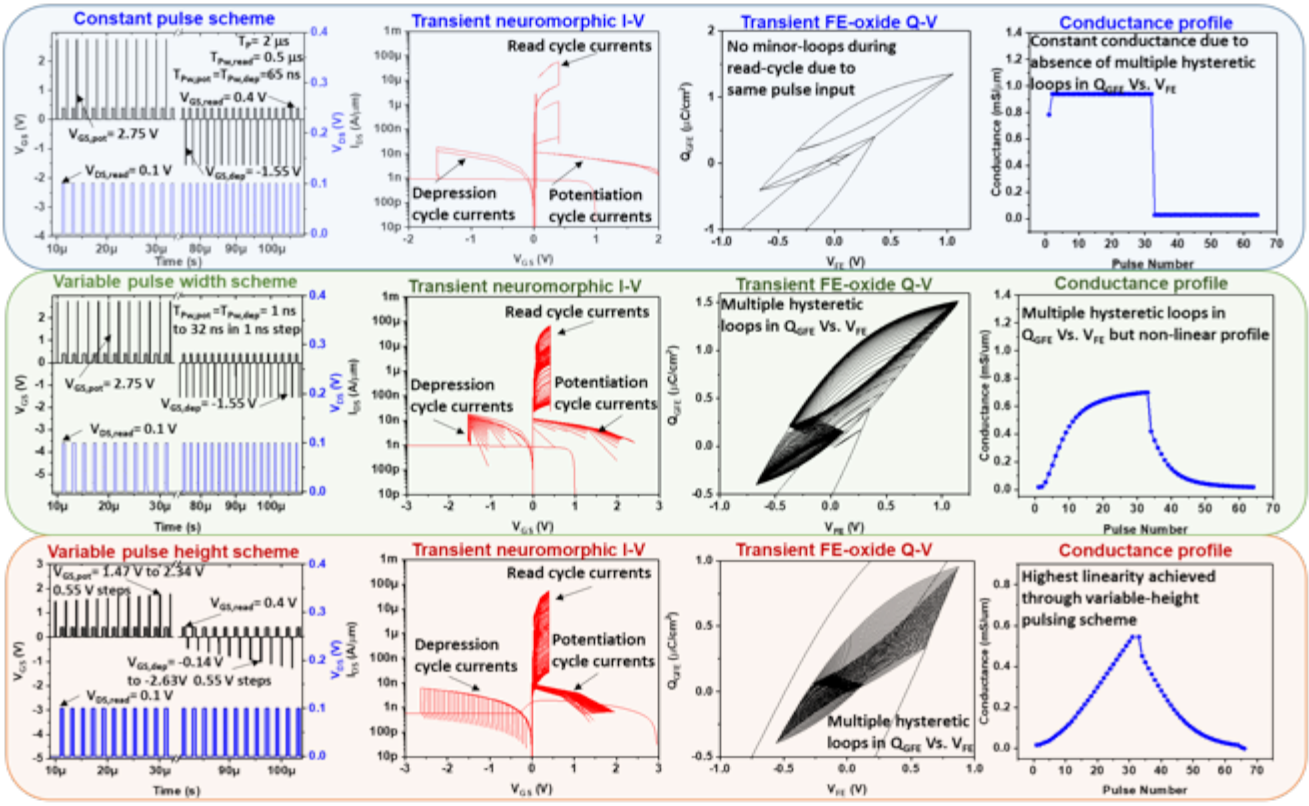


Figure 114 Response of the FeFET synapse is studied for three input (V_G)-pulsing schemes to represent a 5-bit analog synapse: (i) constant potentiation/depression voltage: scheme I. (both in voltage-amplitude and -pulse-width), (ii) ramped-amplitude potentiation/depression voltage: scheme II., and ramped-pulse-width potentiation/depression voltage: scheme III. For each scheme, the simulated transient transfer device-current, Q_{GFE} vs. V_{FE} and the conductance (S, measured in linear region; V_G=0.4 V, V_D= 0.1 V) profile vs. pulse number are shown. In scheme I., the FE-oxide shows no minor-loop behavior in its Q-V which results in square S-response vs. pulse count. In scheme II., the variable V_G-pulse-width results in minor-loop formation, multiple-hysteretic I-Vs and more-linear S-profile. Further improvement in S-profile can be achieved through ramped-amplitude V_G-input as described in [3] which is correctly estimated by the MVSNC modeling framework. The pulse-period (T_p= 2 ns), read-time ($T_{PW,read}$=500 ns), pulse-widths for programming ($T_{PW,pot}$, $T_{PW,dep}$=1-65 ns) and the time-interval between them is chosen such that V_{Gint} has stabilized after programing cycle (and reached zero) before the read-cycle begins ensuring non-volatile state-preservation.

5.3.2 Ferroelectric thickness engineering for improved synaptic characteristics

To further improve the synaptic weight update characteristics, a novel device-engineering technique is proposed as shown in Figure 115. By constructing a composite FeFET that is made of multiple width-elements (fingers) of varying t_{FE} (by 0-12 nm from the nominal value of 10 nm), the Q_{GFE}-V_{GFE} characteristics can be shifted between the constituent elements for the same pulsing scheme as shown. In this scheme, each finger acts as the basis function for parameter tuning for the composite device. This in

turn can improve the on-to-off conductance ratio (G_{max}/G_{min}), by 22% and ~3.7x for scheme II and III respectively as can be seen. Other device-parameters such as V_T, C_{if}/C_{ov} can also be varied along width-direction to study classification-accuracy enhancement using MVSFE framework.

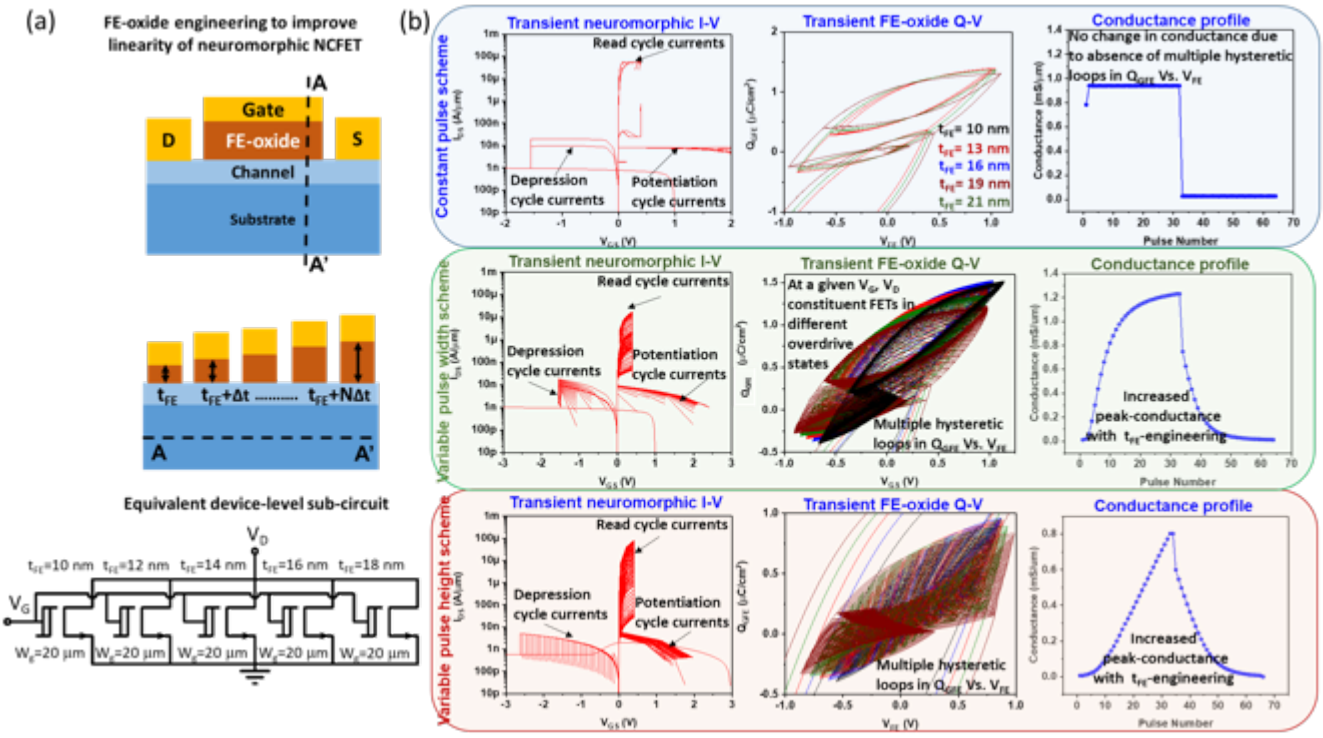
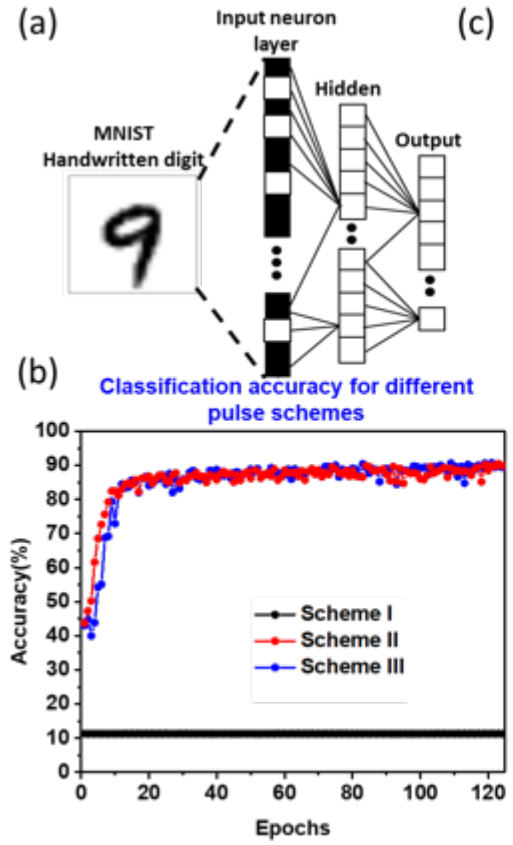


Figure 115(a) To improve the weight update conductance ratio further, a new FeFET synapse architecture is proposed by constructing a device with multiple constituent FET-elements in parallel of equal-width but varying t_{FE} as shown. For the same P_o and E_c, this causes the constituent FETs to respond with different Q_{GFE}-V_{FE} curves as shown for the same inputs as before (Schemes I., II., and III.). In both schemes II. and III the peak-conductance (and hence G_{max}/G_{min}) is improved (by ~2x) as can be seen. The constant-pulse response remains unchanged due to the absence of minor-loops.

5.3.3 Application of highly scaled FeFET in artificial neural network

The engineered device characteristics have been used to determine the classification accuracy of 1 million MNIST handwritten numbers using 2-layer fully connected neural network simulator [196]for three cases. The classification accuracy for case I is at 11% due to the lack of intermediate weight values between on and off states. Scheme III shows ~2% (from ~89% to ~91%) improvement in accuracy when compared to scheme II due to better linearity and G_{max}/G_{min}. The impact of technology scaling along with

the novel device-architecture shows similar accuracy as in [191] while reducing the latency (~ 2×), energy and obtaining active synapse area improvement (~ 100×) excluding the peripheral circuits enabled by dimension scaling compared to earlier works that use longer-channel FeFETs in [191]. It should be noted that nominal device characteristics have been used for system level classification accuracy calculation. Secondary effects like cycle-to-cycle variation may affect the classification accuracy [202].



(c)

Performance metrics	Scheme I	Scheme II	Scheme III
L_g/W_g (nm)	45/5x20	45/5x20	45/5x20
$V_{GS,read}$ (V)	0.4	0.4	0.4
$V_{DS,read}$ (V)	0.1	0.1	0.1
$V_{GS,pot}$ (V)	2.75	2.75	1.47 to 2.34
$V_{GS,dep}$ (V)	-1.55	-1.55	-0.14 to -2.63
T_{PW} (ns)	65	5-160	65
G_{max}/G_{min}	300	47	122
Accuracy after 125 epochs (%)	~11	~88	~90
Area (μm^2)	3489.5	3601.4	3382.5
Latency (s)	0.28	0.97	1.07
Energy (mJ)	1.94	2.11	1.60

Figure 116 (a) The architecture of the multi-layer fully connected (400-100-10) perceptron layer used from MLP Neurosim V2.0 [196] for classification accuracy evaluation of 1 million MNIST handwritten digits. Intel-45 nm node device dimensions and corresponding capacitance values have been used for synapses. (b) Classification accuracy as a function of epochs for different pulse schemes. The improved linearity in scheme III of the proposed composite device has resulted in a better classification accuracy than scheme II. (c) Performance benchmarking for different pulse schemes in terms of accuracy, energy consumption and latency. Highly scaled composite devices show improved G_{max}/G_{min} while maintaining similar classification accuracy as in [191]. All values are calculated using NeuroSim V2.0 [196] which results in significantly lower latency and energy consumption than the values reported in [191] for all NVM devices. Nominal device characteristics have been used (no cycle-to-cycle variation).

5.4 Conclusions

Ferroelectric HfO_2 is very promising materials for many novel applications. We have developed the high quality ferroelectric HfO_2 thin films with various dopants (Al,Si,Zr) and demonstrated application in ultra-lower digital logic devices using negative capacitance effect. Our MoS_2 FET with ferroelectric/dielectric gate stack shows significant improvement in subthreshold swing (SS_{min} ~57 mV/dec) over the control FET (SS_{min} ~67 mV/dec) with standard HfO_2 gate dielectric. This results reveals the potential for ferroelectric HfO_2 in the ultra-low power devices with 2D materials. Moreover, The MVSNC and MVSFE model in Verilog-A (compliant with commercial circuit simulators) developed in this work provides a comprehensive physics-based approach to model FE-oxide-based transistors. It captures various dynamic effects in FE-oxide (such as internal-voltage-amplification, minor-loop formation, memory-wipeout etc.) along with the physics of carrier transport and electrostatics in the underlying MOSFET (such as quasi-ballistic transport, channel-charge partitioning, device-level parasitic-inclusion, device-heating etc.). The model is calibrated against measured state-of-the-art device-characteristics and provides a numerically robust compact modeling framework that can be used by both device- and circuit/system-designers to construct FE-oxide-based transistor circuits.

The usefulness of the model is demonstrated through two example case studies. The model benchmarked against state-of-art RF-HEMTs captures the potential of NCFETs in improving RF- and mm-wave frequency-of-operation along with power-gain enhancement. Additionally, the second example highlights the usefulness of FeFETs as analog synapses along with the benefits of device-engineering and baseline technology node-scaling in artificial neural network applications.

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LIST OF PUBLICATIONS AND CONFERENCE PRESENTATIONS

List of Publications

Van der Waals heterojunction Tunneling

1. **A. Zubair** et al., Hot electron transistors with van der heterojunction base-collector and high performance GaN emitter, **Nano Letters,** 2017, 17 (5), pp. 3089 3096.
2. A. Nourbakhsh, **A. Zubair** et al., *Transport Properties of a MoS_2/WSe_2 Heterojunction Transistor and its Potential for Application*, **Nano Letters**, 2016, 16 (2), pp. 1359-1366.

Ferroelectric gate dielectric Transistors:

3. A. Nourbakhsh, **A. Zubair** et al., *Subthreshold swing improvement in MoS_2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO_2/HfO_2 gate dielectric stack*, **Nanoscale**, 2017, 9, pp. 6122-6127.

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4. A. Nourbakhsh, **A. Zubair** et al., MoS_2 Field-Effect Transistor with Sub-10-nm Channel Length, Nano Letters 2016, 16(12), pp. 7798-7806.
5. A. Nourbakhsh, **A. Zubair** et al., *Sub-10 nm Monolayer MoS_2 FETs with Channel Formed by Directed Self Assembly*, **Symposium on VLSI Technology 2016**, Hawaii, USA

Logic devices with 2D Materials:

6. L. Yu, **A. Zubair** et al., *High- Performance WSe_2 CMOS Technology and Integrated Circuits*, **Nano Letters**, 2015, 15 (8), pp. 4928 4934.
7. L. Yu, D. El-Damak, U. Radhakrishna, X. Ling, **A. Zubair** et al., *Design, Modeling, and Fabrication of Chemical Vapor Deposition Grown MoS2 Circuits with E-Mode FETs for Large-Area Electronics,* **Nano Letters**, 2016, 16 (10), pp. 6349-6356.

Novel 2D materials growth and transfer technology:

8. L. Zhou, **A. Zubair** et al., *Synthesis of High Quality Large Area Homogenous 1T $MoTe_2$ from Chemical Vapor Deposition*, **Advanced Materials**, 2016, 28 (43), pp. 9526-9531.

9. L. Zhou, K. Xu, **A. Zubair** et al., *Large-Area Synthesis of High-Quality Uniform Few-Layer $MoTe_2$*, **Journal of the American Chemical Society**, 2015.
10. J.-Y. Hong, Y.C. Shin, **A. Zubair** et al., *A rational strategy for graphene transfer on substrates with rough features*, **Advanced Materials**, 2016.

List of Conference presentations

1. **A. Zubair** et al., *Negative Capactiance MoS_2 FET with Doped HfO_2 Ferroelectric/dielectric Gate Stack,* **Compound Semiconductor Week** 2018, Boston, MA. (Honorary mention, Best Student Paper Award)
2. **A. Zubair** et al., *MoS_2 FETs with Doped HfO2 Ferroelectric/Dielectric Gate Stack,* **Materials Research Society Fall meeting**, 2018, Boston, MA.
3. **A. Zubair** et al., *Carrier transport studies in Graphene-base Hot Electron Transistor***, American Physical Society March Meeting** 2018, Los Angeles, CA.
4. **A. Zubair** et al., *Graphene-base Hot Electron Transistor with GaN emitter*, **International Conf. on Nitride Semiconductors** 2017, Strasbourg, France.
5. *GaN Hot Electron Transistors Based on a van der Waals Base-Collector Barrier*, **Materials Research Society Fall meeting**, 2017, Boston, MA.
6. **A. Zubair** et al., *Graphene-on-GaN Hot Electron Transistors*, **American Physical Society March Meeting** 2017, New Orleans, LA.
7. A. Nourbaksh, **A. Zubair** et al., *15-nm Channel Length MoS_2 FETs with Single- and Double Gate structures*, **Symposium on VLSI Technology** 2015, Kyoto, Japan, June 2015. (Featured in conference technical tip sheet).
8. **A. Zubair** et al., *Negative Differential Transconductance in a MoS_2/WSe_2 Heterojunction Field Effect Transistor*, **American Physical Society March Meeting** 2015, San Antonio, Texas.
9. **A. Zubair** et al., *Vertical Graphene-base transistor on GaN substrate*, **American Physical Society March Meeting** 2014, Denver, Colorado.
10. A. Nourbaksh, **A. Zubair** et al., *Serially connected monolayer MoS_2 FETs with channel patterned by a 7.5 nm resolution directed self-assembly lithography,* **Symposium on VLSI Technology** 2016, Hawaii, USA, June 2016.

11. P. Wei, **A. Zubair** et al., *Towards valley transistor in MoS_2/EuS through interfacial magnetic exchange field*, **American Physical Society March Meeting** 2017, New Orleans, LA.
12. E. McVay, **A. Zubair** et al., *Fabrication and characterization of multi-layer WSe_2 solar cells,* **American Physical Society March Meeting** 2018, Los Angeles, CA.
13. L. Yu, D. El-Damak, U. Radhakrishna, **A Zubair** et al., *High-yield large area MoS_2 technology: Material, device and circuits co-optimization,* **IEEE International Electron Devices Meeting (IEDM),** 2016.
14. S. Sani, A. Nourbakhsh, A. Devarakonda, **A. Zubair** et al., *Interfacial spin–orbit coupling between two dimensional materials and Thulium Iron Garnet,* **61st Annual Conference on Magnetism and Magnetic Materials,** 2016, New Orleans, LA.

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